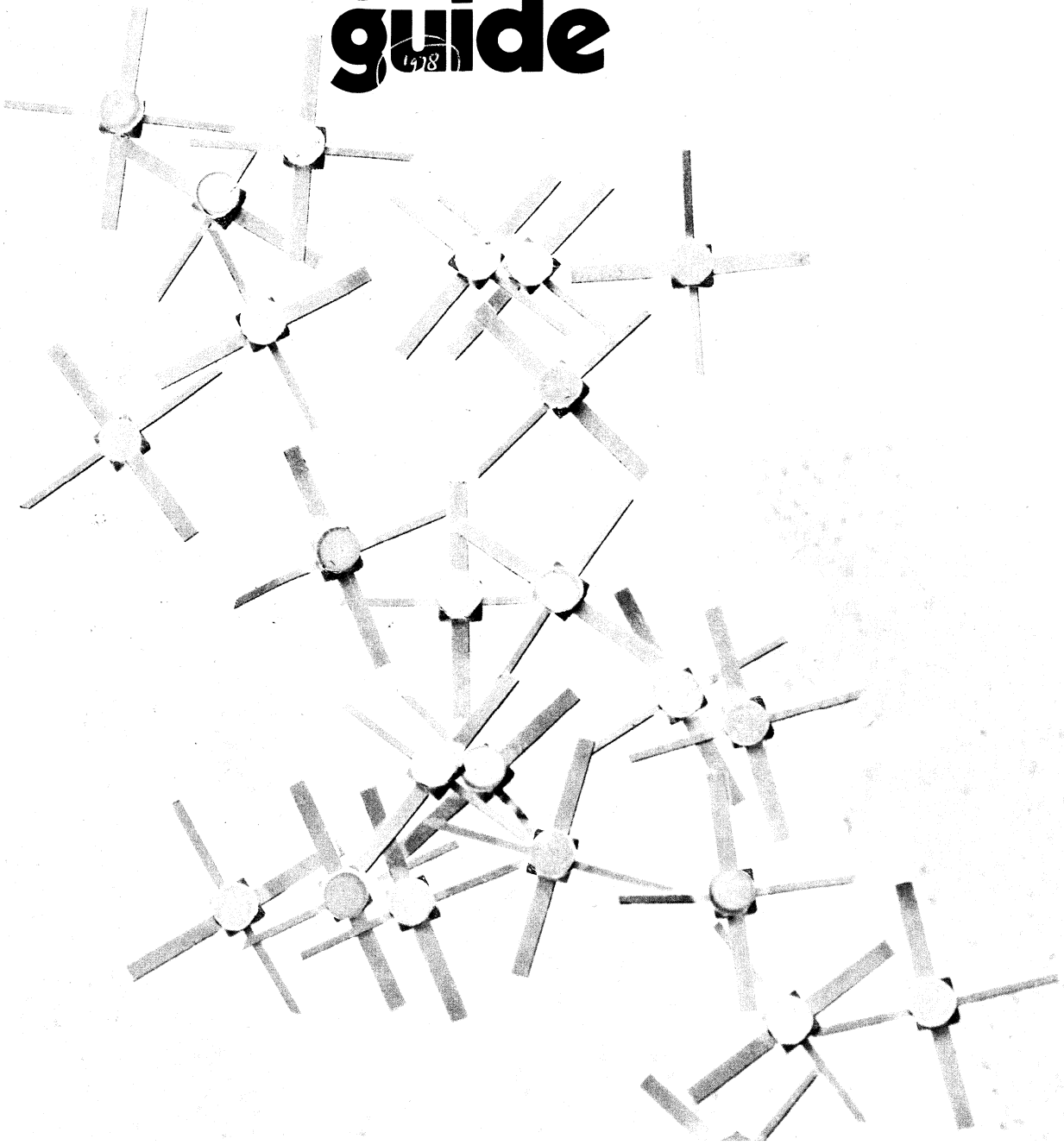
transistor designers guide



introduction

Microwave Associates, the world's largest manufacturer of microwave semiconductor devices, has for over 25 years been developing and manufacturing components using state-of-the-art silicon and gallium arsenide technology for both military and commercial applications.

The Microwave Transistor product represents a high technological level of achievement. This technology is not nearly as flexible as the microwave diode technology which can be readily modified to produce devices to specific customer requirements such as breakdown voltage, capacitance, lifetime and other parameters. The Microwave Transistor product does not lend itself to these options because of the numerous process steps involved. It is for this reason we offer a variety of geometries to fulfill the requirements of our customers for various frequency ranges and applications.

We know that the circuit designer seeks product uniformity. This demands that the components be produced with the tightest of controls and by dedicated production equipment and personnel. This is true whether it be for high volume commercial applications or for high reliability military and space systems. In Burlington, Mass., our ultra modern facility is staffed by a team of dedicated and skilled professionals developing and manufacturing state-of-the-art low noise microwave transistors.

Furthermore, the circuit designer is faced with a multitude of complex design problems and requires that components be well characterized. This Designer's Guide is an outgrowth of our desire to serve these needs of the customer by supplying useful information about the electrical and mechanical characteristics of our products, their applications and their limitations.

We have maintained our technological leadership with a skilled team of technical and marketing specialists who are, and who will be, continually at work providing quality semiconductor products to serve the demanding needs of the industry.

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INTRODUCTION

Most microwave silicon bipolar transistors use the "Planar" process and all are N-P-N. In this process, the critical device dimensions are etched into layers of silicon dioxide. The etched patterns introduced into the oxide layer are called the "geometry" of the transistor. The remaining silicon dioxide is in turn used to mask the wafer against the diffusion of impurities needed to form the active areas.

The type of geometry varies considerably depending upon the application. If power transistors are included, several basic geometries (mesh, overlay, interdigitated) are available, each with its own emphasis on a particular set of design parameters. Since this discussion is restricted to low noise, small signal devices, the preferred geometry is "interdigitated". The term "interdigitated" means that the base and emitter areas appear as interleaved fingers, separated from each other but aligned very close together (see Figure 1). The interdigitated geometry achieves the lowest base resistance without sacrificing gain (or f_{max}). This in turn leads to superior low noise performance. Performance is closely related to wafer processing. To understand performance optimization, it is necessary to understand how a microwave transistor chip is fabricated.

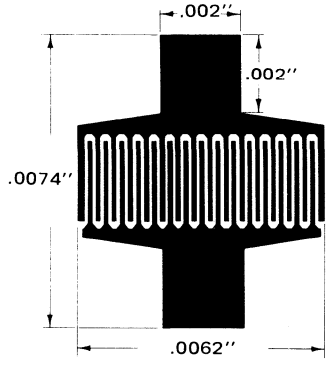

FIGURE 1. INTERDIGITATED GEOMETRY

MICROWAVE TRANSISTOR PROCESSING

The interdigitated structure is best understood by first considering a single transistor cell. A single cell contains one emitter stripe and one base stripe where half of each base stripe is shown on either side of the emitter (Figure 2). The base area ABCD determines the collector-base capacitance. The basic microwave transistor silicon Planar process used to fabricate the cell is illustrated in Figure 3, pg. 2.

Processing begins on an N-type epitaxially grown silicon layer (Figure 3(a), pg. 2) which may have resistivities in the 0.5 to 3 ohm-cm range depending upon the device type. Epitaxial layer thickness ranges from 2 to 5 microns. The epitaxial layer is supported by a heavily doped substrate (not shown) which forms the collector contact.

A thermally grown oxide layer several thousand Angstroms thick is formed on the N-layer surface and the base contact cuts are defined and etched by photo-resist techniques (b).

FIGURE 2(a). SINGLE CELL PLAN VIEW

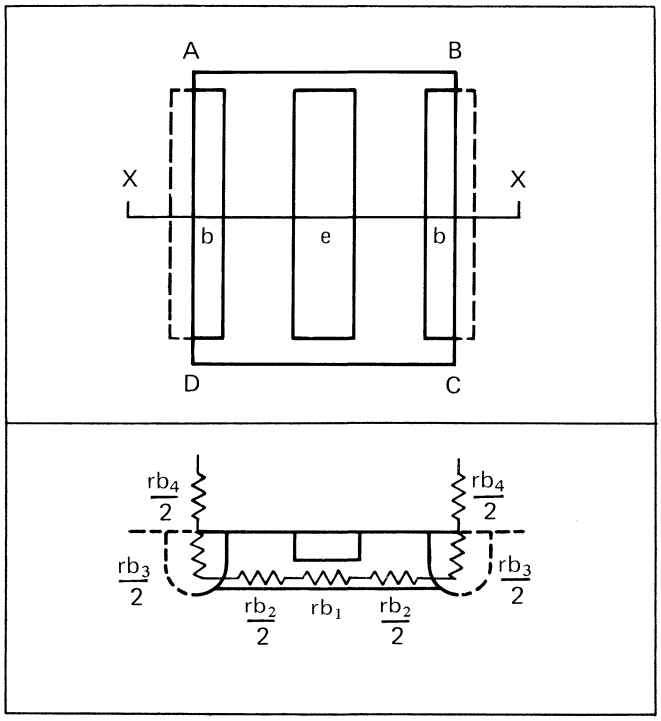

FIGURE 2(b). SINGLE CELL CROSS SECTION THROUGH X-X

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Through the open windows, a heavily doped P-type (Boron) diffusion (P+) is made (Figure 3(c)). This diffusion provides low resistance contacts to the transistor base region. In addition, the high surface concentration lowers the metalization contact resistance.

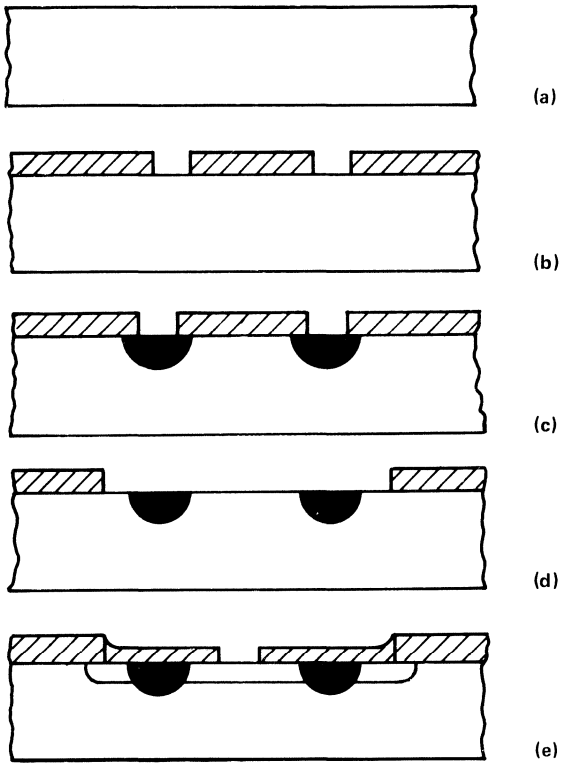
In Figure 3(d), the base area, which encloses all fingers in the finished device, is cut into the oxide. A lightly doped (and precisely controlled) P type diffusion (Boron) is performed through the base area opening (d). The P diffusion forms the transistor base and is automatically connected to the P+ region. During the base diffusion, some oxide growth takes place in the base area. However, it is not usually thick enough to provide for emitter masking. Its thickness is increased by an additional deposition of silicon dioxide.

An emitter opening is defined and etched (Figure 3(e)). This opening is precisely located between the two P+ diffusions.

The transistor is completed by diffusing a shallow, heavily doped N-type emitter into the emitter opening (Figure 3(f)).

In a similar fashion to the base diffusion, a very thin (several hundred Angstroms) oxide appears on top of the diffused emitter. Two types of dopant may be used for the emitter. For low frequencies (<1 GHz) phosphorus is used. For high frequencies (>1 GHz) better performance is achieved with arsenic.

To achieve good microwave performance, the depth of the diffusions are kept very small. The total junction depth of the base of an L-band transistor is only 0.3 micron. The emitter will penetrate only 0.2 micron and the basewidth (the difference between emitter and base junction depths) will be ~0.1 micron. Such shallow diffusions do not obey simple one dimensional solutions to the diffusion equations and in practice, the optimum fabrication conditions are empirically established. Seldom is the exact profile known since very laborious techniques have to be employed in order to determine them. Despite these limitations, continuous refinements in diffusion processing have led to the ability to accurately reproduce profiles once a given high frequency performance has been established.



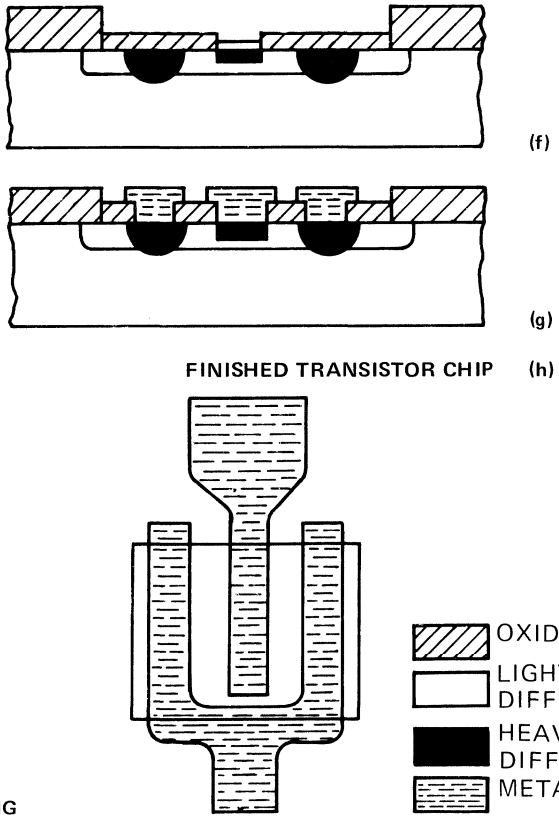


FIGURE 3. TYPICAL MICROWAVE TRANSISTOR WAFER PROCESSING

A typical L-band transistor profile is given in Figure 4. Both arsenic and phosphorous emitter profiles are shown. The extremely sharp emitter gradient of the arsenic profile, as it intersects the base diffusion, results in higher base cutoff frequencies and hence lower noise. It is for this reason that arsenic emitters are widely used to achieve superior microwave performance.

Recently, the more conventional thermal diffusion processes have been replaced by Ion-Implantation. Ion-Implantation is a method of embedding the dopant into a wafer by accelerating the ions toward the wafer with a high electric field. The advantage is that both dopant dose and depth are controlled with much greater precision. Ion-Implantation results not only in greater yield, but superior performance as well.

Contact to the finished transistor is accomplished through metal fingers which have to align with the open P+ and emitter fingers. These openings are made in two steps. First, the emitter oxide is "washed" away by a very short acid etch. Second, the P+ contact opening is defined and etched by photo-resist techniques. The metallization is deposited in a film over the whole wafer area, and the fingers and bonding pads defined by chemical etching. A final cross-section and plan view are given in Figure 3(g) and Figure 3(h), pg. 2, respectively.

During the early development of microwave transistors, aluminum was used as the metallic contact. However, for very shallow junctions, the tendency of aluminum to dissolve the silicon during processing or creep between oxide-silicon interfaces at high temperatures leads to premature emitter-base voltage breakdown or shorts and severely limited yield. Such metallization problems have been eliminated with the advent of refractory gold metalization systems. In these systems, an ohmic contact (platinum silicide) is made to each finger by depositing platinum and reacting it with silicon at high temperature. A refractory layer (titanium-tungsten) is deposited onto the wafer followed by gold. The tungsten prevents the gold from alloying with the silicon under high temperatures (400°C) and the gold allows wire bonding to the refractory layer. In its final form, the structure is very resistant to temperature and forms an extremely reliable device.

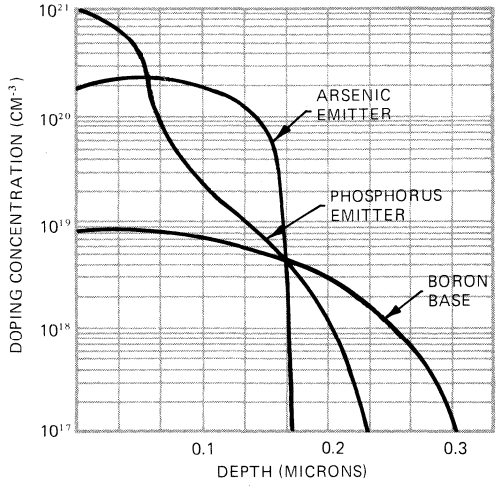


FIGURE 4. TYPICAL L BAND MICROWAVE TRANSISTOR DIFFUSION PROFILE WITH BOTH ARSENIC AND PHOSPHORUS EMITTERS

Once the metallization is complete, the wafer is thinned, to reduce collector series resistance, and scribed to produce individual "chips". Chip size is typically 10-15 mils square and approximately 4 mils thick. Good low resistance contact to the collector is achieved with a gold metallization contact on the back of the chip.

BASIC OPERATION

In order to understand the performance of a microwave bipolar transistor, it is necessary to explain the performance characteristics in terms of key device parameters.

Development of such a theory for packaged microwave transistors requires an analysis of a complicated equivalent circuit model. Such analysis obscures the basic key parameter dependency. A simpler approach is needed. Simplification is best achieved by considering a packageless single cell chip.

A single cell N-P-N transistor is shown in common base configuration in Figure 5. The emitter AB and collector EF

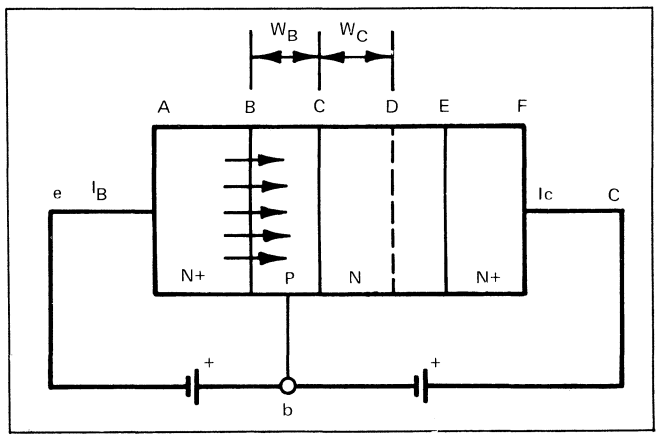


FIGURE 5. COMMON BASE TRANSISTOR OPERATION

are heavily doped N type regions. The base BC and collector CE are moderately doped P and N regions respectively. The biasing network is arranged so that electrons are injected across the emitter-base junction B whereupon they diffuse across the base to the collector. In modern microwave transistors, this diffusion is aided by a drift field in the base due to the doping gradient. Upon reaching the collector C, the electrons are swept across the depletion region CD into the neutral collector circuit DF. Because the basewidth is small, negligible recombination occurs in the base and the common base current gain, α, is given by

$$\alpha = \frac{I_C}{I_E} \approx 1 \qquad (1)$$

The DC base current gain is designated α_o.

In the majority of cases, low noise microwave transistors are used in common emitter configuration because the current gain is higher. The common emitter current gain, β, is related to α by

$$\beta = \frac{I_C}{I_B} = \frac{\alpha}{1-\alpha} \qquad (2)$$

The DC common emitter current gain is designated h_{FE}.

FREQUENCY DEPENDENCE

The variation of $|\alpha|^2$ and $|\beta|^2$ as a function of frequency is shown in Figure 6. At low frequencies, $|\beta|^2$ is equal to the dc current gain $|h_{FE}|^2$. As frequency increases, a point is reached where it begins to decline at a rate of 6dB per octave until it reaches unity. The frequency at which β is equal to unity ($|\beta|^2 = 0$dB) is designated f_T. Similarly, the frequency at which α reaches 0.707 α ($|\alpha|^2 = -3$dB) is designated f_α. Both f_T and f_α play a key role in determining the power gain and noise figure characteristics. High frequency transistors operate in the frequency range where β is not equal to its low frequency value.

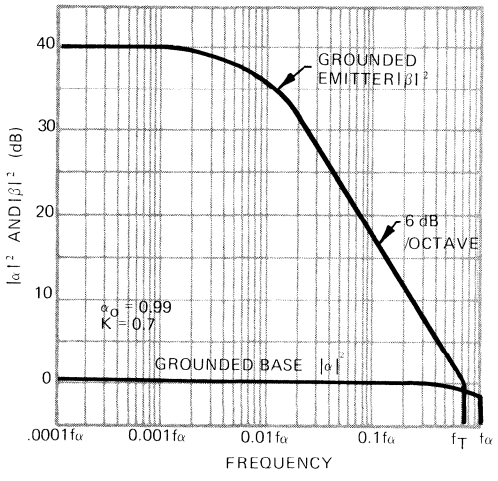


FIGURE 6. FREQUENCY DEPENDENCE OF $|\alpha|^2$ AND $|\beta|^2$

POWER GAIN AND MAXIMUM FREQUENCY OF OPERATION

The maximum small signal power gain at a given frequency, f, if the single cell is conjugately matched at both input and output, is

$$G_{max} = \frac{f_T}{8\pi f^2 r_B C_C} \qquad (3)$$

where

r_B = base resistance

C_C = collector capacitance

The frequency at which G_{max} is unity is called the maximum frequency of oscillation or f_{max}.

$$f_{max} = \left(\frac{f_T}{8\pi r_B C_C}\right)^{1/2} \qquad (4)$$

Thus, the higher the f_T the higher the gain at a particular frequency. However, to optimize gain, both r_B and C_C must simultaneously be reduced.

BASE RESISTANCE

The base resistance is composed of the sum of four parts as illustrated in Figure 2(b), pg. 1. The magnitude of each contributing resistance depends upon the base and P+ doping profiles and the geometry dimensions.

A fair approximation of their values is given by

$$r_{b1} = \frac{R_1 S}{12 L} \qquad (5)$$

$$r_{b2} = \frac{R_2 S}{2 L} \qquad (6)$$

$$r_{b3} = \frac{R_3 S}{12 L} \qquad (7)$$

$$r_{b4} = \frac{R_C}{L S} \qquad (8)$$

where

r_{b1} = resistance of the intrinsic base

r_{b2} = resistance of the extrinsic base

r_{b3} = resistance of the P+ region

r_{b4} = contact resistance to the base

S = stripe width

L = stripe length

R_1 = base sheet resistance under emitter

R_2 = base sheet resistance between emitter and base

R_3 = sheet resistance of P+

R_c = specific contact resistance of metal — P+ contact

Thus, the total base resistance r_B for a unit cell becomes

$$r_B = r_{b1} + r_{b2} + r_{b3} + r_{b4} \quad (9)$$

NOISE FIGURE

The noise figure of a transistor is a measure of the degradation of the signal-to-noise ratio as the signal is processed by the device. This degradation occurs because of the presence of three noise sources within the chip itself. These noise sources are shot noise due to current flow in the emitter-base and collector circuits and thermal noise generated by the base resistance r_B.

Noise figure is not a simple function of the device parameters. Furthermore, it is dependent on the input and output impedances presented to the chip with the input source impedance playing the dominant role.

For a particular current and frequency, there exists a noise figure minimum for an optimum value of source impedance. Under these circumstances

$$NF_{min} = 1 + \frac{r_B}{Rg_{opt}} + \frac{r_e}{2Rg_{opt}} + \frac{(Rg_{opt} + r_B + r_e)^2}{2\,\alpha_o r_e\, Rg_{opt}} \left[\left(\frac{f}{f\alpha}\right)^2 + \frac{1}{h_{FE}}\right] \quad (10)$$

where

r_B = base resistance

Rg_{opt} = optimum source impedance

r_e = dynamic resistance of the emitter

f = operating frequency

The variation of minimum noise figure with frequency according to Equation (10) is shown in Figure 7.

Initially, in the "plateau" region, NF_{min} remains relatively constant up to a frequency, f_p, beyond which it increases asymptotically to a 6dB/octave slope.

Most UHF transistors operate in the plateau region while microwave transistors operate between f_p and f_c.

While Equation (10) depicts the correct trend, it is never used to characterize transistors, because both f_α and r_B cannot be measured other than through noise figure measurements. Instead, all transistors are thoroughly characterized at several frequencies using very accurate noise figure measurement techniques.

CUT-OFF FREQUENCIES

Both f_T and f_α profoundly influence noise figure and current gain. Their dependency upon geometry and diffusion profiles becomes apparent if the operation of the cell is analyzed with respect to the delays occuring as a signal passes through it. It is intuitively easier to visualize if common-base operation is considered first. The signal encounters four successive delays:

(1) Emitter Delay:

$$\tau_E = r_e C_{TE} = \frac{kT}{q\, I_E} C_{TE} \quad (11)$$

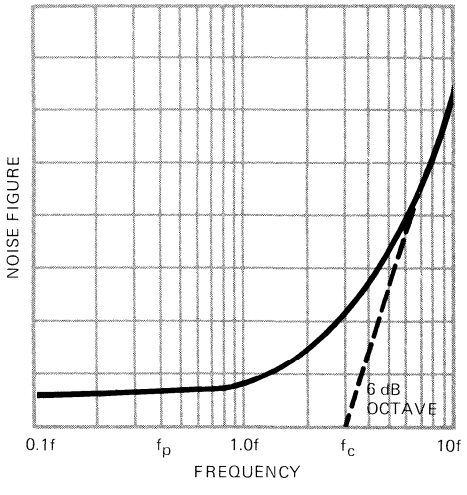


FIGURE 7. NOISE FIGURE AS A FUNCTION OF FREQUENCY

where

r_e = dynamic emitter resistance
C_{TE} = emitter transition capacitance
I_E = emitter bias current
q = electronic charge
k = Boltzmann's constant
T = absolute temperature °K

The emitter delay is due to the time it takes for the emitter capacitance to charge through the emitter resistance.

(2) Base Transit Delay:

$$\tau_B = \frac{W^2}{2.45\, D\, \eta} \qquad (12)$$

where

W = basewidth

D = average diffusivity of injected electrons in base

η = factor which accounts for the reduction of τ_B due to the base diffusion profile

The base delay is caused by the finite time injected electrons take to travel across the base region.

(3) Collector Transit Time:

$$\tau_S = \frac{X_D}{2V_{SC}} \qquad (13)$$

where

X_D = collector depletion width

V_{SC} = saturation drift velocity in collector epitaxial layer

The collector transit delay is the time taken for the electrons to travel across the collector depletion layer.

(4) Collector Delay:

$$\tau_{coll} = r_C C_C \qquad (14)$$

where

r_C = collector series resistance

C_C = collector capacitance

The collector delay is the time taken to charge the collector through the collector series resistance.

The total delay is given by adding the four delay times which defines the alpha cut-off frequency:

$$\frac{1}{2\pi f_\alpha} = \tau_E + \tau_B + \tau_S + \tau_{coll} \qquad (15)$$

Furthermore, since f_α and f_T are related by

$$f_\alpha \approx K\, f_T \qquad (16)$$

f_T can be determined if the constant K is known. K is a constant largely determined by the usually unknown base impurity profile.

PERFORMANCE OPTIMIZATION

Broadly speaking, performance optimization means increasing f_T and f_α and lowering r_B.

Increasing f_T or f_α means reducing each delay time. This amounts, in practice, to the following:

(a) Reduce emitter widths, which reduces the emitter capacitance.

For low noise operation up to 1 GHz, S ~ 2.5 microns. For operation between 1 - 4 GHz, S has to be steadily decreased to a micron. Micron linewidths represent the limit of the optical photolithographic process.

(b) Reduce basewidth W. (Limited by ability to sustain BV_{CEO}.)
(c) Keep collector epitaxial layer as thin as possible. (Limited by ability to sustain BV_{CBO}.)
(d) Choose collector epitaxial layer resistivity and thickness to maximize V_{sat}.
(e) Reduce C_C by minimizing base area ABCD, Figure 2. However, the base area must be large enough to comfortably contain the emitter and base fingers.
(f) Reduce r_C by using low resistivity substrate. (Typically 0.01 ohm-cm.)
(g) Increase η by using shallow, steep impurity gradients for both emitter and base diffusions. This approach eventually demands the control achievable only with Ion-Implantation.

In addition, noise figure can be improved by simultaneously reducing base resistance. Steps (b) and (g) will also improve base resistance, but further improvements occur if

(h) the length of each finger is increased. This is limited by the potential drop that occurs down the stripe. If the drop is large enough, it will result in de-biasing of the extreme portions of the emitter. For this reason, the ratio of strip length to width is kept below 25:1, and
(i) single cells are combined in parallel.

The total base resistance R_B becomes

$$R_B = \frac{1}{N} r_B \qquad (17)$$

where N = number of emitters.

Actually, single cells as depicted in Figure 2, pg. 1 seldom appear as a finished product since even with the outlined dimensions, base resistance remains too high; but lowering r_B by connecting cells in parallel has limitations. Since emitter area increases, cutoff frequency declines (at low currents), thus the paralleling of cells is eventually limited by a marked reduction in low current gain. The trade-offs involved have led to a proliferation of interdigitated geometries each with its own unique set of characteristics.

(j) In the plateau region, noise figure can be lowered by increasing h_{FE}. This is a particularly useful technique for designing low noise UHF transistors.

PACKAGED TRANSISTORS

Connection to the outside world (package) is aided by metal bonding pads on the chip. They are isolated from the substrate by an oxide layer but are positioned as close to the cell as practical. Since the substrate to bond pad capacitance is undesirable, pads are kept to a minimum size consistent with the ability to bond wires to them. One to two mils square is typical. The bond pads are connected to the fingers to give the familiar plan view of a typical low noise geometry as shown in Figure 1, pg. 1.

Once a transistor is packaged, the RF performance becomes modified by the parasitic inductances and capacitances involved. Bonding pads on the chip add extra capacitance, bonding wires constitute additional inductances and the package adds both capacitance and inductance to the circuit. As a result power gain may not fall at 6dB/octave, but at a smaller rate. Near f_T resonances may occur, particularly at higher frequencies. The current gain may always be greater than one so that f_T is not well defined. The optimum source impedance for minimum noise will differ from that required by the chip alone. However, minimum noise figure is usually not affected by package parasitics. To illustrate these effects, the measured $|\beta|^2$ of the MA42001 is given in Figure 8 as a typical example of the packages effected upon gain.

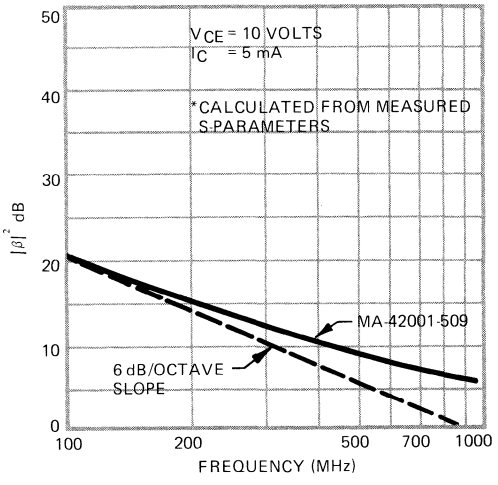


FIGURE 8. VARIATION OF MEASURED* $|\beta|^2$ WITH FREQUENCY FOR MA-42001 IN 509 PACKAGE

amplifier design

The use of the S or scattering parameters has gained almost universal acceptance in the characterization of microwave transistors. The reason for this acceptance becomes apparent when considering the termination requirements for the other popular characterization parameters for transistors, namely the h, y and z parameters. When using these parameters to characterize a network it is necessary that the input and/or output be short-circuited and/or open-circuited. Consider the h-parameters. For this illustration we will assume that the network has 2 ports; an input port and an output port as shown in Figure 1.

The equations relating the network's input/output characteristics when using h-parameters are the following:

$$V_1 = h_{11} I_1 + h_{12} V_2 \quad (1)$$

$$I_2 = h_{21} I_1 + h_{22} V_2 \quad (2)$$

Normally, when using parameter sets to characterize a network, either the port voltages or the port currents are selected as independent variables and the port current or the port voltages are then dependent variables. In the case of the "h" or hybrid parameters I_1 and V_2 are selected as the independent variables and V_1 and I_2 then are the dependent variables.

As can be seen from Eq. (1), h_{11} can be measured if the input port is excited with a voltage V_1 and the output port is short-circuited, $V_2 = 0$.

$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2 = 0} \quad (3)$$

Also, h_{12} can be measured if the output port is excited with a voltage V_2 and the input port is open-circuited ($I_1 = 0$).

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1 = 0} \quad (4)$$

In a similar manner h_{21} and h_{22} can be determined.

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2 = 2} \text{ and } h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1 = 0} \quad (5)$$

The short and open circuit conditions required for these measurements must appear as short and/or open circuits at the port being terminated. At high frequencies this requirement can be quite difficult to obtain since any length of transmission between the port and the termination (short or open) will cause the impedance seen by the port to appear to be a reactance. Using the transmission line equation it can be shown that a short circuit terminating a length of line will appear as a reactance determined by equation 6.

$$Z_S = +j Z_O \tan\left(\frac{2\pi\ell}{\lambda}\right) \quad (6)$$

where λ is the wavelength at the measuring frequency and the remaining terms are as shown in Figure 2.

This expression (Eq. 6) shows that the impedance Z_S, will be inductive if ℓ/λ is .25 or less and will approach a short circuit only if ℓ/λ approaches zero.

It can also be shown that an open circuit terminating a length of line will appear as a reactance as determined by Equation 7.

$$Z_S = -j Z_O \operatorname{cotan}\left(\frac{2\pi\ell}{\lambda}\right) \quad (7)$$

In this case if ℓ/λ is less than .25, the Z_S will be capacitive and only approach an open circuit if ℓ/λ approaches 0.

Equations 6 and 7 also show that when ℓ/λ is .25 that the **short** circuit equivalency of equation 7 appears as an **open** circuit, and the **open** circuit condition of equation 7

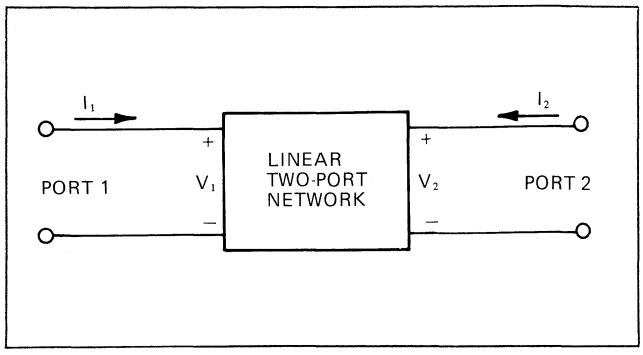


FIGURE 1. TWO PORT NETWORK

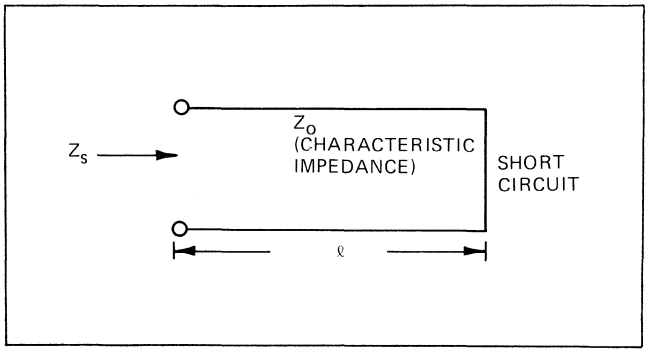


FIGURE 2. TRANSMISSION LINE TERMINATED BY A SHORT CIRCUIT

appears as a **short** circuit. It becomes apparent from the preceeding discussion, that broadband short and open circuits will be difficult to obtain at high frequencies. The network also may be unstable and oscillate under these conditions if the network is active.

It is primarily for these reasons that S-parameter characterization is presently being used to characterize transistors. When using S-parameters, both the input and output ports at all times are terminated in the characteristic impedance of the measuring system (normally 50 ohms). Under these conditions, the network will generally be stable and not oscillate.

While h, y and z parameters utilize input/output currents and voltages to characterize the network, S-parameters use travelling waves, the variables being the normalized incident and reflected complex voltage waves for each port of the network. (Figure 3.)

The term a_i is defined as the normalized incident voltage wave and b_i is defined as the normalized reflected voltage wave.

$$a_i = \frac{V_i + Z_i I_i}{2\sqrt{R_e Z_1}} \tag{8}$$

$$b_i = \frac{V_i + Z_i^* I_i}{2\sqrt{R_e Z_i}} \tag{9}$$

where

V_i = terminal voltage
I_i = terminal current
Z_{i_*} = reference impedance
Z_i^* = complex conjugate of the reference impedance.

Generally Z_i is a positive real impedance and is set equal to Z_o, the characteristic impedance of the measuring system. Equations (8) and (9) then simplify to:

$$a_i = \frac{V_i + I_i Z_o}{2\sqrt{Z_o}} \tag{10}$$

$$b_i = \frac{V_i - I_i Z_o}{2\sqrt{Z_o}} \tag{11}$$

If the a_i variables are set to be the independent variables and the b_i variables to be the dependent variables, then the following set of equations can describe the network:

$$b_1 = S_{11}\, a_1 + S_{12}\, a_2 \tag{12}$$

$$b_2 = S_{21}\, a_1 + S_{22}\, a_2 \tag{13}$$

These equations can be graphically represented by the use of a signal flow graph wherein each port of the network will be represented by 2 nodes. The a_i nodes will represent the travelling wave entering the device at the i^{th} port and the b_i node will represent the travelling wave leaving the network at the i^{th} port. From inspection of Eq. (12) and (13) it then becomes apparent that the various scattering parameter coefficients essentially represent the effects of waves entering various ports on the wave leaving a particular port.

Figure 4 is the signal flow graph representation of Eqs. (12) and (13).

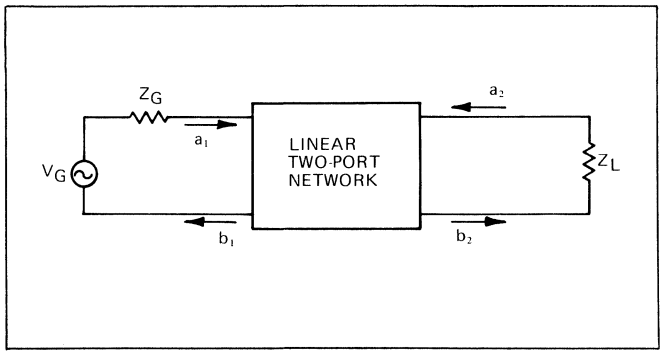


FIGURE 3. COMPLEX VOLTAGE WAVE REPRESENTATION FOR A LINEAR TWO-PORT NETWORK

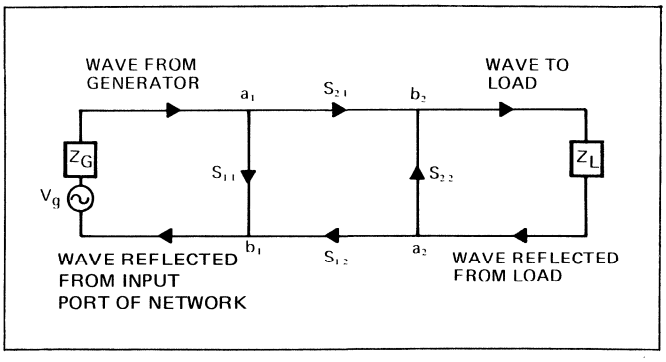


FIGURE 4. SIGNAL FLOW GRAPH FOR A LINEAR TWO-PORT NETWORK

To solve Eqs. (12) and (13) for the various scattering coefficients it is necessary to set the a_1 terms to zero. From the signal flow graph (Figure 4, pg. 10) to set a_2 to zero it is necessary to have no wave reflected from Z_L, the load. This can be achieved by having $Z_L = Z_o$. To set a_1 to zero, there must be no wave emenating from the generator. To do this $V_g = 0$ and $Z_G = Z_o$. The S-parameters are:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2 = 0} \equiv \frac{\text{voltage wave reflected from port 1}}{\text{voltage wave incident on port 1}} \quad (14)$$

$\equiv$ Input reflection coefficient with the output port terminated in Z_o

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1 = 0} \equiv \frac{\text{voltage wave reflected from port 2}}{\text{voltage wave incident on port 2}} \quad (15)$$

$\equiv$ Output reflection coefficient with the input port terminated in Z_o

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2 = 0} \equiv \frac{\text{voltage wave reflected (or leaving) port 2}}{\text{voltage wave incident (or centering) port 1}} \quad (16)$$

$\equiv$ Forward transmission coefficient with the output port terminated in Z_o

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1 = 0} \equiv \frac{\text{voltage wave reflected (or leaving) port 1}}{\text{voltage wave incident (or returning) port 2}} \quad (17)$$

$\equiv$ Reverse transmission coefficient with the input port terminated in Z_o

Referring to Eqs. (10) and (11), important significance of the scattering parameters can be seen:

$$S_{11} = \frac{b_1}{a_1}\bigg|_{a_2 = 0} = \frac{\dfrac{V_1 - I_1 Z_o}{2\sqrt{Z_o}}}{\dfrac{V_1 + I_1 Z_o}{2\sqrt{Z_o}}} = \frac{\dfrac{V_1}{I_1} - Z_o}{\dfrac{V_1}{I_1} + Z_o} \quad (18)$$

$$= \frac{Z_{in} - Z_o}{Z_{in} + Z_o}$$

where Z_{in} is the input impedance of the network with the output port terminated in Z_o.

$$S_{22} = \frac{b_2}{a_2}\bigg|_{a_1 = 0} = \frac{\dfrac{V_2 - I_2 Z_o}{2\sqrt{Z_o}}}{\dfrac{V_2 + I_2 Z_o}{2\sqrt{Z_o}}} = \frac{\dfrac{V_2}{I_2} - Z_o}{\dfrac{V_2}{I_2} + Z_o} \quad (19)$$

From inspection of Eqs. (18) and (19) the input and output impedance of the device can be calculated once S_{11} and S_{22} are known. Since S_{11} and S_{22} are reflection coefficients they can also be plotted on Smith charts.

Continuing with the above discussion:

$$S_{21} = \frac{b_2}{a_1} \equiv \frac{\text{voltage wave leaving port 2}}{\text{voltage wave entering port 1}} \equiv \left[\frac{\text{power leaving port 1}}{\text{power entering port 1}}\right]^{1/2} \quad (20)$$

$$S_{12} = \frac{b_1}{a_2} \equiv \frac{\text{voltage wave leaving port 1}}{\text{voltage wave entering port 2}} \equiv \left[\frac{\text{power leaving port 1}}{\text{power entering port 2}}\right]^{1/2} \quad (21)$$

Equations (20) and (21) show that $|S_{21}|^2$ and $|S_{12}|^2$ are the network's forward and reverse gain when the network is embedded in a system with Z_o source and load.

amplifier design
GAIN

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If the S-parameters of a network are known, several meaningful relationships can be determined. Normally, signal flow graphs in conjunction with the set of rules established for using signal flow graph analysis are used to determine these relationships. The rigorous use of signal flow graphs has been well described in the literature (1, 2, 3) and is beyond the scope of this note. However, we will describe in general terms how they can be used.

As stated before, Figure 4, pg. 10 is the signal flow graph of a two port network and it will be used for the following discussion. In the design of amplifiers, it is desirable to know the effect of loading the network with arbitrary generator and load impedances (i.e., the effect on gain, input impedance and output impedance).

As can be seen from Figure 4, pg. 10 if ZL = Zo then the wave reflected from the load is zero and the input reflection coefficient of the network is simply

$$S_{11}' = S_{11} = \frac{b_1}{a_1} \tag{22}$$

If

$$Z_L \neq Z_o, \text{ then}$$

$$S_{11}' = \frac{b_1}{a_1} = S_{11} + \frac{S_{21}\, S_{12}\, \Gamma_L}{1 - S_{22}\, \Gamma_L} \tag{23}$$

where

$$\Gamma_L = \frac{Z_L - Z_o}{Z_L + Z_o}$$

In a similar manner, S_{22}' the output reflection coefficient with arbitrary Z_G can be determined.

$$S_{22}' = S_{22} + \frac{S_{21}S_{12}\, \Gamma_S}{1 - S_{11}\, \Gamma_S} \tag{24}$$

where

$$\Gamma_S = \frac{Z_G - Z_o}{Z_G + Z_o}$$

Equation (23) shows the effect of load impedance on the reflection coefficient of the network and therefore on the input impedance. If the $S_{21}S_{12}$ product in the second form of (23) is minimized the load impedance effects on input impedance will be minimized. The above discussion can also be applied to Eq. (24) with respect to source (generator) impedance effects on the output impedance of the network.

The "$S_{21}S_{12}$" factor in both equations (23) and (24) appear in several characteristic equations. This factor is a determinant for stability and input/output isolation.

S_{11}' and S_{22}' can be plotted directly on a Smith chart to gain information about the input and output impedances of the network. The input and output impedance can be calculated by using:

$$Z_{in} = Z_o \left(\frac{1 + S_{11}'}{1 - S_{11}'} \right) \tag{25}$$

$$Z_{out} = Z_o \left(\frac{1 + S_{22}'}{1 - S_{22}'} \right) \tag{26}$$

Transducer power gain (G_T) can also be determined using signal flow graph techniques.

$$G_T = \frac{\text{Power Absorbed by the Load}}{\text{Power available from the generator}} = \frac{P_{abs}}{P_{avg}} \tag{27}$$

P_{abs} = P (incident on the load) − P (reflected from the load)

$$P_{abs} = |b_2|^2 \, (1 - |\Gamma_L|^2)$$

$$P_{avg} = \frac{|b_g|^2}{(1 - |\Gamma_L|^2)}$$

$$G_T = \left| \frac{b_2}{b_g} \right|^2 (1 - |\Gamma_g|^2)\,(1 - |\Gamma_L|^2)$$

$$\frac{b_2}{b_g} = \frac{S_{21}}{(1 - S_{11}\,\Gamma_g)\,(1 - S_{22}\,\Gamma_L) - S_{21}S_{12}\Gamma_g\Gamma_L}$$

$$G_T = \frac{|S_{21}|^2\,(1 - |\Gamma_g|^2)\,(1 - |\Gamma_L|^2)}{|(1 - S_{11}\,\Gamma_g)\,(1 - S_{22}\Gamma_L) - S_{21}S_{12}\Gamma_L\Gamma_g|^2} \tag{28}$$

where b_g is the normalized generator voltage.

Equation (28) can be simplified if S_{12} is assumed to be zero. The transducer gain is then:

$$G_{Tu} = \frac{|S_{21}|^2 \ (1 - |\Gamma_g|^2)\ (1 - |\Gamma_L|^2)}{(\ |1 - S_{11}\Gamma_g|^2)(|1 - S_{22}\Gamma_L|^2)} \quad (29)$$

where G_{Tu} is the unilateral transducer power gain.

The question arises as to the accuracy of this expression in determining the gain of the network. A figure of merit can be determined by solving for the ratios of G_T/G_{Tu}. The maximum error will be

$$\frac{1}{(1+U)^2} < \frac{G_T}{G_{Tu}} < \frac{1}{(1-U)^2} \quad (30)$$

where U is the unilateral figure of merit

$$U = \frac{|S_{11}S_{12}S_{21}S_{22}|}{(1 - |S_{11}|^2)\ (1 - |S_{22}|^2)} \quad (31)$$

Figure 5 shows the variation of $\frac{G_T}{G_{Tu}}$ in dB as a function of U. As can be seen, an error of less than 1.0 dB in $\frac{G_T}{G_{Tu}}$ can be obtained if U is less than approximately 0.11.

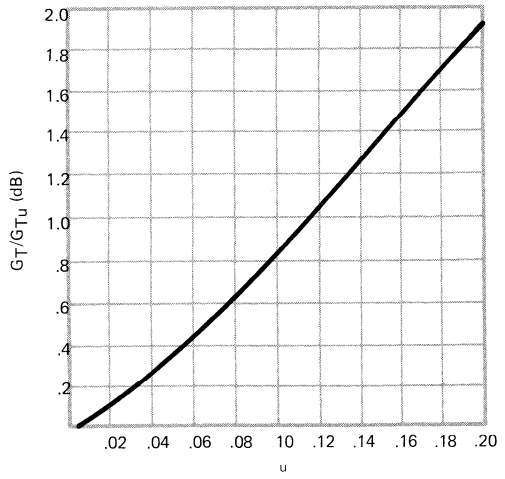

FIGURE 5. UNILATERAL FIGURE OF MERIT VS UNILATERAL GAIN CALCULATION ACCURACY

Once it has been established that the unilateral expression for gain is sufficiently accurate, the RF design of the amplifier becomes relatively straight forward.

Equation (29) can be rewritten as shown in equation 31.

$$G_{Tu} = |S_{21}|^2 \bullet \frac{(1 - |\Gamma_g|^2)}{|1 - S_{11}\Gamma_g|^2} \bullet \frac{(1 - |\Gamma_L|^2)}{|1 - S_{22}\Gamma_L|^2} \quad (32)$$

Equation (32) shows that the unilateral transducer power is composed of 3 terms, each independent of the other. The first term, $|S_{21}|^2$, is unique to the transistor bias and frequency sensitivity. The gain contribution from the second term, $\frac{(1 - |\Gamma_L|^2)}{|1 - S_{11}\Gamma_g|^2}$ is related only to the input matching of the transistor while the third term, $\frac{(1 - |\Gamma_L|^2)}{|1 - S_{22}\Gamma_L|^2}$ is related only to the output matching.

Unilateral transducer gain can be maximized by choosing impedance matching networks such that $\Gamma_g = S_{11}^*$ and $\Gamma_L = S_{22}^*$. Equation 32 then becomes

$$G_{Tu}max = |S_{21}|^2 \bullet \frac{1}{1 - |S_{11}|^2} \bullet \frac{1}{1 - |S_{22}|^2} \quad (33)$$

Circles of constant gain can be plotted on a Smith chart showing the effect on gain when changing either Γ_g or Γ_L. These circles result from the solutions to the second and third terms of equation (32), and are determined by the following equations:

R_i = The radius of the constant gain circle

$$R_i = \frac{\sqrt{1 - gi}\,(1 - |S_{ii}|^2)}{1 - |S_{ii}|^2\ (1 - gi)} \quad (34)$$

di = The distance from the center of the Smith chart to the center of the constant gain circle:

$$di = \frac{gi\ |S_{ii}|}{1 - |S_{ii}|^2\ (1 - gi)} \quad (35)$$

G_i = gain represented by the constant gain circle.

$$g_i = G_i\ (1 - |S_{ii}|^2) = \frac{G_i}{G_{i\,max}} \quad (36)$$

Each circle has its center located on the vector drawn from the center of the Smith chart to the point S_{11}^* or S_{22}^*.

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Figures 6 and 7 show the constant gain circles for input and output impedance match, respectively, of a typical 1 GHz transistor. The transistor chosen for this example is the MA-42141-511. Typical S-parameters for the transistor at 1 GHz and V_{CE} = 10 volts, I_C = 5 mA are:

S_{11}	.594	$\angle -162.3°$
S_{21}	3.628	$\angle 75.2°$
S_{12}	.058	$\angle 32.4°$
S_{22}	.592	$\angle -39.5°$

Using equation (33) the maximum unilateral transducer gain is 14.88 dB with the input matching term contributing 1.81 dB, the output matching term contributing 1.81 dB, and the $|S_{21}|^2$ term contributing 11.19 dB.

Although the preceeding discussion addresses gain at a single frequency, complete gain characterization for a device may be obtained by calculating the gain values at several frequencies within the desired range.

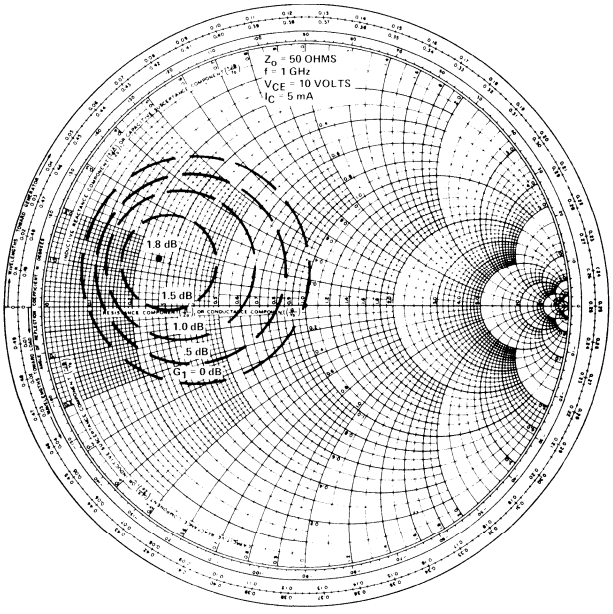

FIGURE 6. MA-42141-511 CIRCLES OF CONSTANT GAIN AS A FUNCTION OF INPUT IMPEDANCE TERMINATION

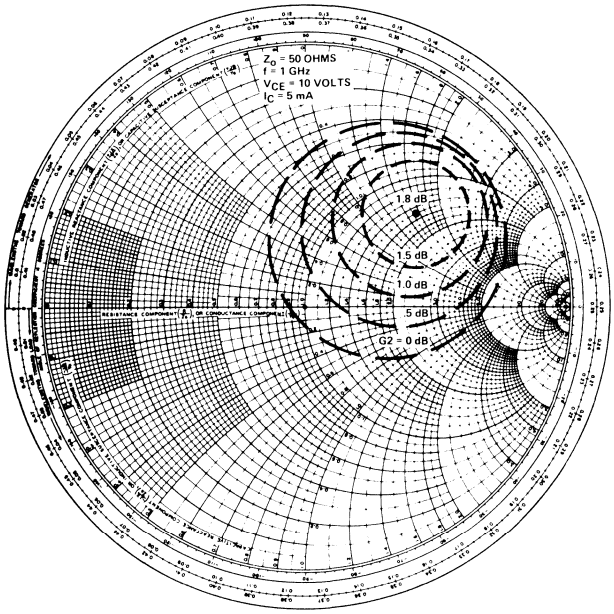

FIGURE 7. MA-42141-511 CIRCLES OF CONSTANT GAIN AS A FUNCTION OF OUTPUT IMPEDANCE TERMINATION

An important factor, which should not be neglected in amplifier design, is whether the amplifier is stable for the matching conditions and whether there are any input or output loading conditions which would cause the amplifier to oscillate.

An amplifier is unconditionally stable at a specified frequency if the real part of its input and output impedances is positive for any positive real input and output terminations. The implication of this statement is that there are no conditions, when using passive loading, for the amplifier to oscillate. Since the real part of the amplifier's input and output impedances must be positive, then the input and output reflection coefficients of the amplifier are less than one.

$$s_{11}' = s_{11} + \frac{s_{21}\, s_{12}\, \Gamma_L}{1 - s_{22}\, \Gamma_L} \leqslant 1 \qquad (37)$$

$$s_{22}' = s_{22} + \frac{s_{21}\, s_{12}\, \Gamma_S}{1 - s_{22}\, \Gamma_S} \leqslant 1 \qquad (38)$$

Referring to equation(37)if $\Gamma_L = \Gamma_O = 0$ then, s_{11} must be less than or equal to one for unconditional stability. In a similar manner, in equation (38) if $\Gamma_S = \Gamma_O = 0$, then it can be seen that $s_{22} \leqslant 1$ for unconditional stability.

Rollett's stability factor, K, takes into account that s_{11}', s_{22}', s_{11} and s_{22} must all be less than or equal to one for unconditional stability. For this condition $K > 1$, Rollett's stability factor from equations (37) and (38) (Ref. 1) is:

$$K = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta|^2}{|2\ s_{21} s_{12}|} \qquad (39)$$

Where $\Delta = s_{11} s_{22} - s_{21} s_{12}$.

An amplifier is conditionally stable at a specified frequency if the real part of its input and output impedances is positive for some positive real input and output terminations. This means that for some positive real input and output terminations s_{11}' and/or s_{22}' will be greater than one. Therefore K, Rollett's stability factor, will also be less than one.

When considering an amplifier design which is conditionally stable, it is possible to map out on a Smith Chart the locus of all values of Γ_S or Γ_L that will cause the amplifier to oscillate and determine the range of loading on the input and output for stability.

By setting $s_{11}' = 1$ or $s_{22}' = 1$ in equations (37) and (38) respectively the boundary between stable and potentially unstable regions can be established. Then, the solutions to equations (37) and (38) form circles in the reflection coefficient plane.

The circle will be located at a distance, r_{s1}, given by

$$r_{s1} = \frac{C_2^*}{|s_{22}|^2 - |\Delta|^2} \qquad (40)$$

from the center of the Smith Chart.

The radius of the circle is given by:

$$R_{s1} = \left| \frac{|s_{12}\, s_{21}|}{|s_{22}|^2 - |\Delta|^2} \right| \qquad (41)$$

where

$$C_2^* = (s_{22} - \Delta s_{11}^*)^*$$

The asterisk (*) denotes the complex conjugate of the quantity.

Similarly, we obtain from equation (38) by setting $s_{22}' = 1$, the solution for Γ_S in the reflection coefficient plane. Or,

$$r_{s2} = \frac{C_1^*}{|s_{11}|^2 - |\Delta|^2} \qquad (42)$$

$$R_{s2} = \left| \frac{|s_{12}\, s_{21}|}{|s_{11}|^2 - |\Delta|^2} \right| \qquad (43)$$

$$C_1^* = (s_{11} - \Delta s_{22}^*)^*$$

Now, as an example, we will apply these results for a specific transistor — MA 42141 in an ODS-511 stripline package.

Figure 8 shows the input and output stability circles for the MA-42141-511 when operating at 1 GHz and V_{CE} = 10 volts, I_C = 5 mA.

Once the stability circles have been established, it is then necessary to determine whether the area inside the circle is the stable or unstable region. Consider the input stability circle. The stable region on the Smith Chart will be that region where $s_{11}' < 1$ (Ref. Eq. 37) . If Γ_L in Eq. (37) is set equal to zero, then s_{11}' will equal s_{11}. If $s_{11} < 1$ then the point on the Smith Chart where $\Gamma_L = 0$ is located in the stable operating region. This point ($\Gamma_L = 0$) is the center of the Smith Chart. In a similar manner the stability region for the output can be determined (i.e. Set $\Gamma_S = 0$).

In the case of the stability circles shown in Figure 8, the stable region for the input and output is that portion of the Smith Chart not encircled by the stability circles.

Figure 9 shows the relative positions of the constant gain and stability circles for the unilateral matching conditions previously shown in Figures 6 and 7, pg. 14. This data indicates the network is stable over a large range of matching conditions. The stability of an amplifier design should be investigated over a broad range of frequencies and stability circles determined at those frequencies.

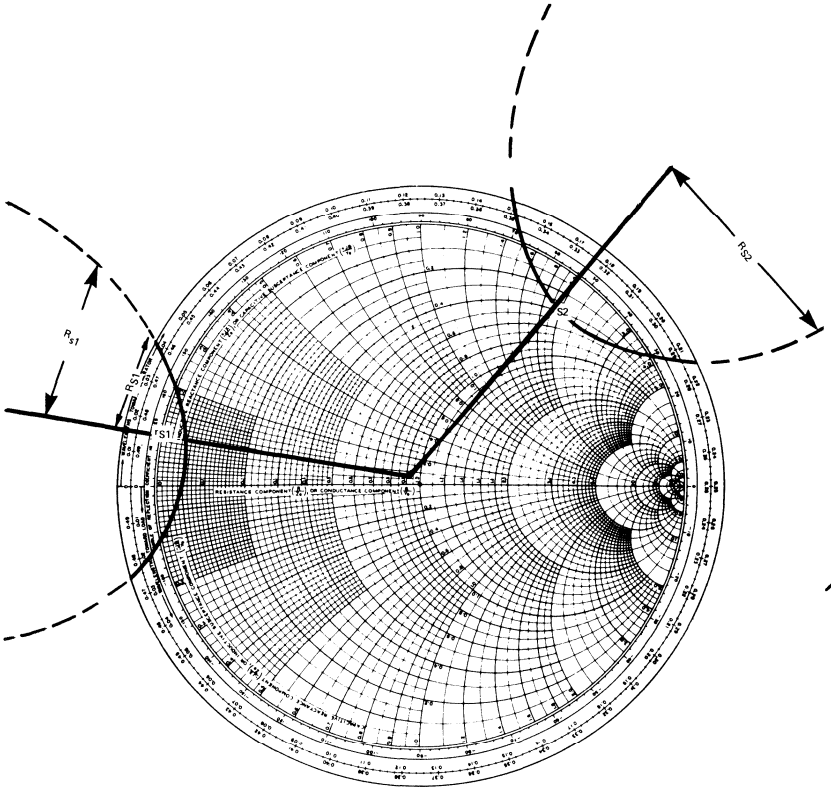

FIGURE 8. INPUT AND OUTPUT STABILITY CIRCLES @ 1 GHz FOR THE MA-42141-511.

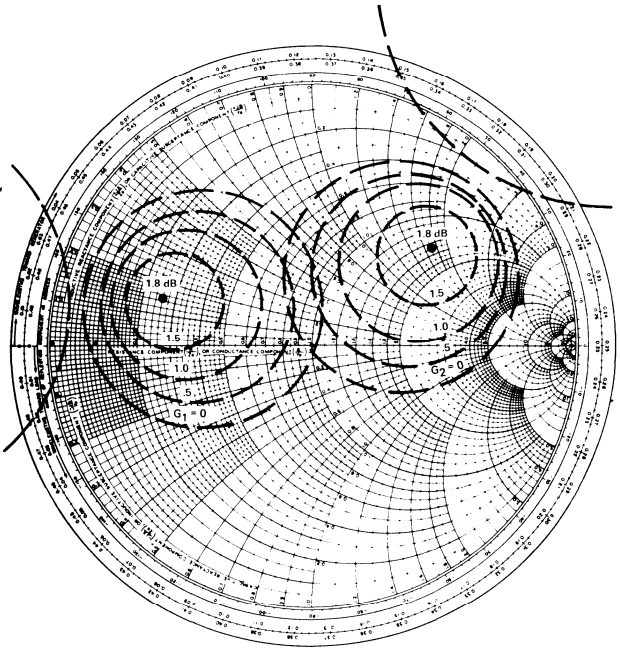

FIGURE 9. CONSTANT GAIN AND STABILITY CIRCLES

A plot of stability factor versus frequency for various transistors shows that the transistor will be conditionally stable over most of the transistor's useful frequency range. This is illustrated in Figure 10 where stability factor has been plotted for 4 different types of transistors. The increase seen in stability factor versus frequency can be mainly attributed to the change in the "$s_{21}\ s_{12}$" factor in the denominator of the equation for stability factor (Eq. 39). "s_{21}", the forward gain is decreasing at approximately 6 dB per octave. "s_{12}", the reverse gain, which is predominately a feedback capacitance effect, is increasing with frequency. The net effect of these changes is shown in Figure 11, where $|s_{21}\ s_{12}|^2$ vs frequency is plotted for the MA-42161-511 transistor. This curve shows that this parameter is essentially constant at the lower usable frequencies and then decreases at approximately 2 dB/octave at the higher frequencies. This characteristic is generally true for all transistors.

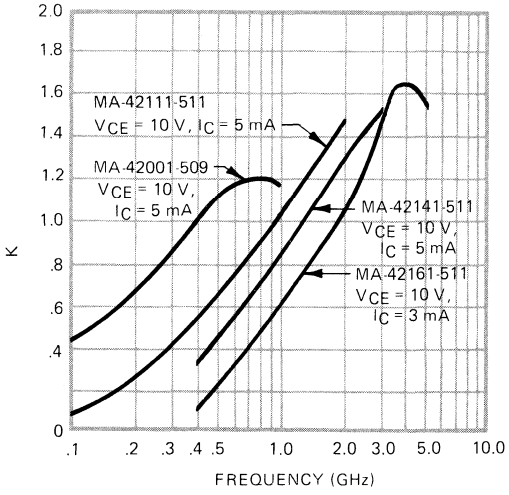

FIGURE 10. STABILITY FACTOR VS FREQUENCY

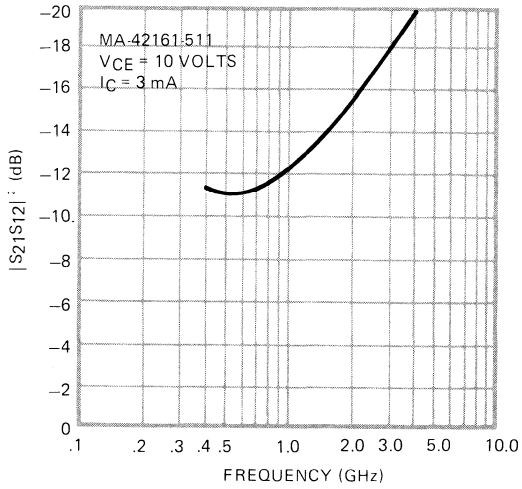

FIGURE 11. $|S_{21}S_{12}|^2$ (dB) VS FREQUENCY

amplifier design

NOISE FIGURE

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The design of low noise transistor amplifiers no longer requires empirical techniques if the transistor being considered has been characterized for certain noise parameters. The use of these noise parameters is described in the following test.

It has been established[1,3] that the noise figure of a linear two-port will vary with source admittance as shown in Equation (44).

$$F = F_{opt} + \frac{R_n}{G_s}\left[(G_{opt} - G_s)^2 + (B_{opt} - B_s)^2\right] \qquad (44)$$

where R_n is the noise resistance factor

F_{opt} is the optimum noise figure

$G_{opt} + jB_{opt}$ is the source admittance at optimum noise figure conditions

$G_s + jB_s$ is the source admittance

in terms of source reflection coefficient Eq. (44) becomes

$$F = F_{opt} + 4R_n \frac{|\Gamma_s - \Gamma_{opt}|^2}{(1 - |\Gamma|^2)(1 + |\Gamma_{opt}|^2)} \qquad (45)$$

where Γ_s and Γ_{opt} are respectively the reflection coefficients of the source admittances in Eq. (44)

The solution to this equation for noise figure as a function of source reflection coefficient is a family of circles of constant noise figure. The center of the circles on the Smith Chart is found by the following:

$$C_{Fi} = \frac{\Gamma_{opt}}{1 + N_i} \qquad (46)$$

where $$N_i = \frac{F_i - F_{opt}}{4R_n}\left|1 + \Gamma_{opt}\right|^2$$

F_i = the value of the noise figure associated with the i th circle.

The radius of the circle can be determined by:

$$R_{Fi} = \frac{(N_i^2 + N_i\,|\Gamma_{opt}|^2))^{1/2}}{1 + N_i} \qquad (47)$$

Normally the number of circles to be calculated is a set of 5 or 6 chosen for convenience and clarity.

Table I lists the typical noise parameters for three Microwave Associates transistors as characterized for low noise operation. D.C. operating conditions for the MA-42161-511 are V_{CE} = 10 volts, I_C = 3 mA, while the MA-42141-511 and MA-42111-511 operate at V_{CE} = 10 volts, I_C = 5 mA.

Freq. (GHz)	MA 42161			MA 42141			MA 42111		
	Γ_{opt}	R_n	F_{min} (dB)	Γ	R_n	F	Γ_{opt}	R_n	F_{min}
.450	– –	– –	– –	.34 +40°	.39	1.8 dB	.25 +115°	.58	1.4 dB
1.0	.29 +64°	1.34	1.4	.30 +93°	.58	2.2 dB	– –	– –	– –
2.0	.33 +142°	.338	2.3	.37 +162°	.30	4.0 dB	– –	– –	– –

TABLE 1. TYPICAL NOISE PARAMETERS FOR LOW-NOISE TRANSISTORS

Figure 12 depicts a family of constant noise figure circles for the MA-42141-511 transistor when operated at 1 GHz. This data shows that the transistor noise figure is fairly insensitive to small source-reflection coefficient changes when operating near the optimum source reflection coefficient.

Figure 13 indicates the tradeoffs that the circuit designer must face. Both constant noise figure and constant gain circles are shown together, to graphically describe the many matching combinations possible.

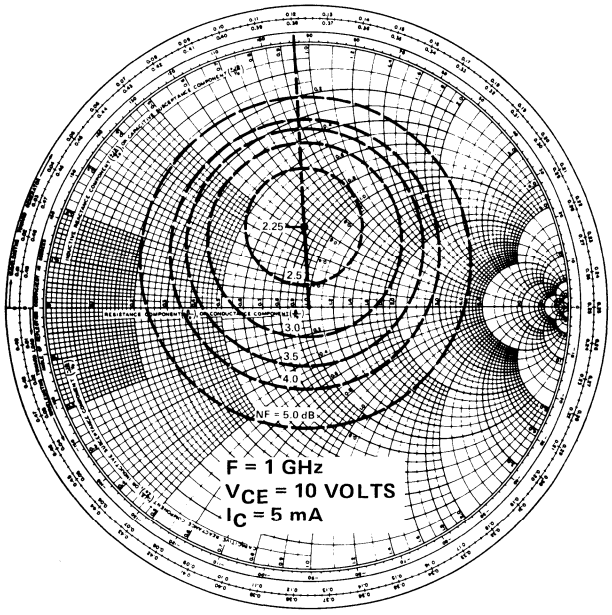

FIGURE 12. CONSTANT NOISE FIGURE CIRCLES FOR THE MA-42141-511.

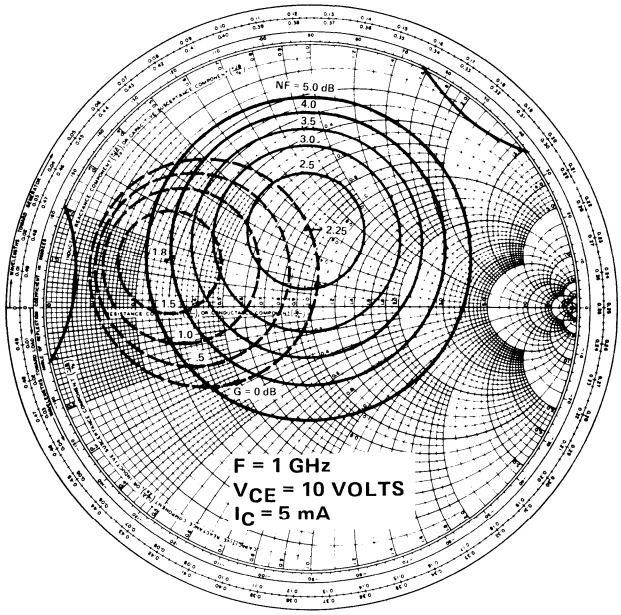

FIGURE 13. CONSTANT GAIN CIRCLES SUPERIMPOSED ON CONSTANT NOISE FIGURE CIRCLES FOR THE MA-42141-511.

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With a transistor amplifier and a receiver arranged as shown in Figure 14, transistor noise figure can be calculated using the relationship:

$$NF_{Tr} = NF_{system} - \left(\frac{F_{rcvr} - 1}{G_{trans}}\right) \quad (48)$$

NF_{Tr} = transistor noise figure

NF_{system} = noise figure of the overall system

F_{rcvr} = receiver noise figure

G_{trans} = transistor gain

Since the transistor is embedded in the test circuit, a thorough knowledge of the effects of the various components in the test circuit on the circuit's noise figure is required. Figure 15 shows a typical noise system used for the measurement of Noise Figure at 2 GHz. The use of a filter is required to eliminate any image frequency (2.120 GHz) effects during the measurement. The elimination of the filter can cause an apparent lower noise figure. The isolator preceeding the 3.8 dB post amplifier reduces the effect of tuning the transistor on the gain and noise figure of the post amplifier. This isolator (Microwave Associates MJ2-1500) has an input VSWR of 1.02:1 and an isolation of 32 dB at 2 GHz. The receiver is defined as all those components following the output of the transistor.

During the measurement of the receiver noise figure, the stub in the coaxial slide screw tuner is fully extracted, eliminating the tuner's effect on line impedance.

Since any losses preceeding the transistor input will add linearly in dB to the measured noise figure, the insertion losses of the bias tee and the tuner are measured at 2 GHz. (Again the coaxial tuner's stub is fully extracted.) This loss is subtracted from the excess noise of the solid-state noise source.

The solid-state noise source is calibrated by the manufacturer with traceability to the National Bureau of Standards. This calibration was verified at Microwave Associates by comparing measured noise figure using the solid-state noise source and a hot-cold noise generator. The results were within ± .15 dB. This verification was also used to confirm the NF reading made with the AIL Type 7380 noise system monitor.

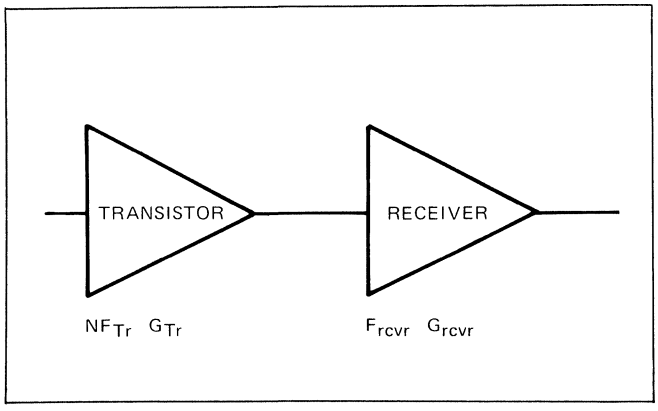

FIGURE 14. TRANSISTOR AND RECEIVER AS USED IN A TYPICAL NOISE MEASUREMENT

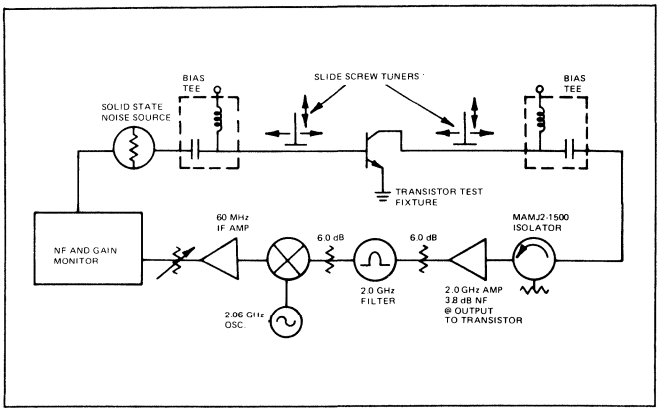

FIGURE 15. 2 GHz NOISE FIGURE TEST SYSTEM

Once these precautions (calibrations) have been completed, the system noise figure can be measured at optimum source conditions by use of the tuners. The source reflection coefficient presented to the transistor can be determined by disconnecting the input tuner, bias tee and solid-state noise source from the transistor and measuring the reflection coefficient of the combination and correcting for the electrical length of the transistor test fixture from the input connector to the base of the transistor.

Figure 16 shows the effect of the collector current on the optimum noise figure of a typical MA-42161 transistor at 2 GHz.

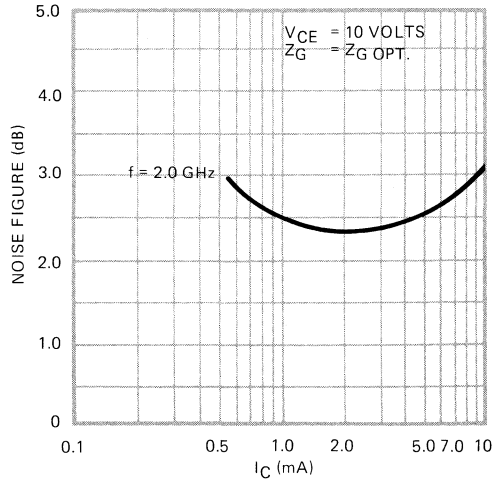

FIGURE 16. TYPICAL NOISE FIGURE VS COLLECTOR CURRENT

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TRANSISTOR AMPLIFIER DYNAMIC RANGE

The dynamic range of a transistor amplifier is defined as the input power limits over which the amplifier has useful gain. The concept of what is "useful" gain is somewhat arbitrary and depends on the specific circuit application in which the transistor will be used. However, over the years some standard definitions of dynamic range have evolved for the purpose of characterizing transistors.

The low power limit for useful gain will be determined by the background noise level of the amplifier. The high power limit depends on whether the amplifier is used for a single frequency signal or for amplifying several frequencies simultaneously. For the single frequency amplifier, the upper limit of dynamic range will be determined by the gain compression characteristic of the transistor. For the multiple frequency amplifier, the upper limit of dynamic range will be determined by the power level of the intermodulation signals relative to the primary signal. Each limit of dynamic range will be discussed in detail.

LOWER INPUT POWER LIMIT

Any transistor amplifier will have a noise background at the input. The transistor cannot normally be used unless the output signal can be detected above the noise background. It is reasonable to define a minimum detectable input signal as 3 dB above the background noise or

$$P_{min} = N_{input} + 3\ dB \qquad (49)$$

where P_{min} is the minimum input power in dBm at which the transistor may be used and N_{input} is the input noise in dBm. We may express the input noise as

$$N_{input} = 10 \log \left[\frac{(kTB)}{1\ mW}\right] + NF\ in\ (dB) \qquad (50)$$

where the first term represents the thermal noise and the second term represents the amplifier noise figure. In equation (50) k is Boltzmann's constant, T is the temperature in degrees Kelvin, B is the system bandwidth in Hz. Equations (49) and (50) may be combined to give

$$P_{min} = 111\ dBm + 10 \log B + NF \qquad (51)$$

where B, is the amplifier bandwidth in MHz. Equation (51) shows the minimum power level of a transistor amplifier is dependent on the amplifier bandwidth and the transistor noise figure. An increase in bandwidth by a factor of 10 increases the minimum input signal required by 10 dBm.

UPPER INPUT POWER LIMIT

Single frequency case.

The power output of a transistor is related to the power input by the gain, that is

$$G = 10 \log\left(\frac{P_{out}}{P_{in}}\right) \qquad (52)$$

where G is the power gain of the transistor in dB and P_{out} and P_{in} are the output and input powers, respectively, of the transistor. Equation (52) states that if the gain is constant, the output power will always be G dB greater than the input power. Saturation effects at high input power levels cause the gain to decrease in actual transistors. The input power at which the gain departs from a constant varies with each transistor design. It is customary to specify the input power at which the gain is reduced by 1 dB as a standard parameter for transistors. This input power level is called the 1 dB compression point. Figure 17 shows the P_{out} versus power in for a typical transistor. The dotted line shows the ideal constant gain relationship between output and input power. Note that this line has a slope of

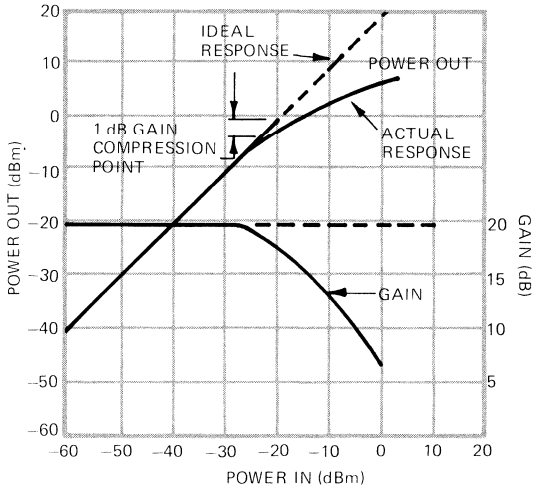

FIGURE 17. POWER OUT VS POWER IN AND GAIN FOR A TYPICAL TRANSISTOR WITH 20 dB GAIN SHOWING 1 dB COMPRESSION POINT

1 on our graph. The solid line shows the actual transistor response. The 1 dB compression point is identified in the figure. Table 2 shows the typical 1 dB gain compression power levels for the various models of Microwave Associates transistors.

UPPER INPUT POWER LIMIT

Multiple frequency case.

When multiple frequency signals, for example, F_1 and F_2 are present at the input to a transistor, the nonlinearities of the transistor will generate spurious responses which are at the single and multiple sum and difference frequencies of the input signals. The bandwidth of the amplifier will determine whether or not the various spurious responses are harmful to the system. As the input signals increase in power, the nonlinearities and generation of spurious responses increase. The presence of the spurious responses imposes an upper limit on the input power at which the system can be used. For some systems the transistor is useful so long as spurious responses are 30 dB below the primary response.

For others, any detectable spurious response is unacceptable. For this reason it is difficult to give absolute power limits to the problem of intermodulation products. It is preferred to give relations between the primary signals and the spurious response which the user can then utilize to derive meaningful power limits for his application. One of the best treatments of the power levels of intermodulation products has been given by F. McVay in Electronics Design, Vol. 3, February, 1967.

Listed below are the signals which are of concern in any intermodulation problem:

Primary Signal	f_1, f_2	These are the signals which the amplifier is intended to amplify without distortion.
Second order products	$2f_1, 2f_2, f_1 + f_2, f_1 - f_2$	These are normally of concern only to very broad band amplifiers. They usually fall outside the bandwidth of the amplifier.
Third order products	$2f_1 + f_2, 2f_1 - f_2, 2f_2 - f_1, 2f_2 + f_1$	The most troublesome ones are $2f_1 - f_2$ and $2f_2 - f_1$ which will normally always fall in the amplifier bandwidth.

MODEL NUMBER	N.F. (MAX)	GAIN (MAX)	TEST FREQUENCY (MHz)	OUTPUT POWER 1 dB COMP PT AT OPTIMUM NF (TYPICAL)
MA42001	1.0 dB	27 dB	60	0 dBm
MA42005	2.0 dB	30 dB	60	+19 dBm
MA42010	3.5 dB	20 dB	450	+27 dBm
MA42025	2.5 dB	13 dB	450	−10 dBm
MA42051	2.0 dB	15 dB	450	−10 dBm
MA42111	1.5 dB	19 dB	450	0 dBm
MA42123	2.3 dB	13 dB	450	−10 dBm
MA42141	2.5 dB	16 dB	1000	0 dBm
MA42161	2.5 dB	14 dB	2000	− 5 dBm
MA42181	5.0 dB	14.5 dB	1000	+25 dBm
2N2857, JAN	4.5 dB	21 dB	450	−10 dBm
2N6665	1.0 dB	27 dB	60	0 dBm

TABLE 2. VALUES OF 1 dB GAIN COMPRESSION POWER LEVELS FOR MICROWAVE ASSOCIATES TRANSISTORS

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Examination of the expansion in a power series of the non linearity which causes the intermodulation products shows that the primary signal is proportional to the input signal amplitude, the second order products are proportional to the input signal amplitude squared, and the third order products are proportional to the cube of the input signal amplitude. Thus, if one were to plot the power level of each output signal on a log-log plot or dB versus dB plot, the primary, second order, and third order signals would have slopes of 1, 2, and 3 respectively. At the normal operating power levels of the transistor, the second and third order intermodulation products are well below the fundamental or primary signals. However, because of the increased slope of the second and third order products, the projected lines of primary, second order and third order signal power out versus primary input power will intersect. The intersection point is normally well above the normal useful range of the transistor. The intercept points of primary, second order and third order signal power becomes the most convenient way to characterize the transistor amplifier for intermodulation effects.

Figure 18 illustrates the technique for determining the power level of the various intermodulation signals. For a given transistor, the 1 dB gain compression output power is a known quantity from the data sheets. Then using the gain of the transistor stage, a curve of primary power out versus primary power in can be drawn. This will be a straight line of slope 1. Our measurements have shown that the intercept point of the third order products is usually 11 dB above the 1 dB gain compression point for our transistors. In determining the power level of the intermodulation products, the highest power signal in the input signal spectrum should be used as the power in value. Thus, the intercept and slope (slope = 3) of the third order products is known. This line can be drawn directly on the figure. Our measurements have shown that, as a worst case approximation, the intercept point of the second order intermodulation products is at the same point as the third order. In most cases, it is at least 5 to 10 dB higher than the third order intercept point. The second order intermodulation products are usually of little consequence since the signals are normally out of the bandwidth of amplification. As a worse case approximation, the second order intermodulation signals can be drawn with a slope of 2 intersecting at the same point, that is 11 dB above the 1 dB gain compression point. With the three lines on the figure, one can then predict the power levels of the intermodulation products which are of concern to his application. This will, in turn, lead to a maximum input power limit to the dynamic range of the transistor.

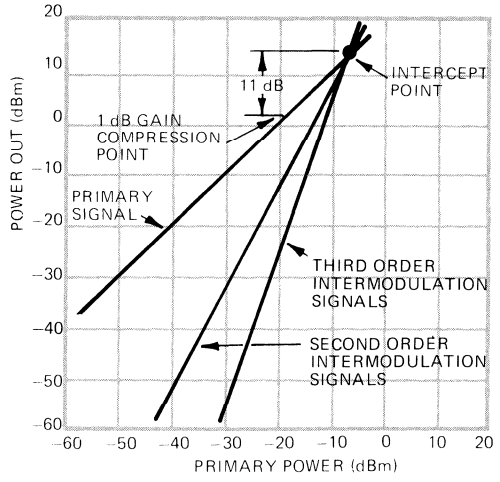

FIGURE 18. OUTPUT POWER OF PRIMARY, SECOND ORDER INTERMODULATION, & THIRD ORDER INTERMODULATION SIGNALS VS PRIMARY INPUT POWER SHOWING INTERCEPT POINT

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2. Bodway, G.E., Two Port Power Flow Analysis Using Generalized Scattering Parameters, Microwave Journal, Vol. 10, No. 6, May 1967.
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amplifier design examples

amplifier design examples

30 MHz PREAMPLIFIER

The I-F preamplifier circuit described below offers a very low noise figure and a bandwidth of 10 MHz. This particular design was introduced to improve the system performance of the popular Microwave Associates Gunnplexer Transceiver for X-Band Applications. Specific design objectives were to minimize the overall system noise figure and to provide suitable gain to overcome cable losses between the mixer-preamp location and the 30 MHz I-F stage.

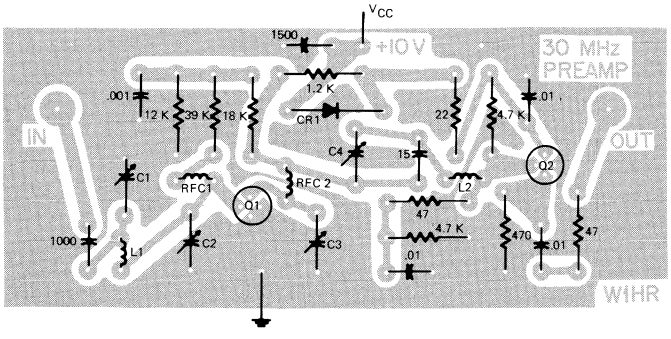
The output impedance of the Gunnplexer Mixer is typically 200 ohms. The input circuitry of the preamplifier has been optimized for the lowest noise figure for this source impedance by computer-aided design techniques. The output portion of this amplifier utilizes an emitter follower which provides a constant 50 ohm load for the following stage (30 MHz I-F Amplifier). This forced 50 ohm condition assures stability of the amplifier under most conditions.

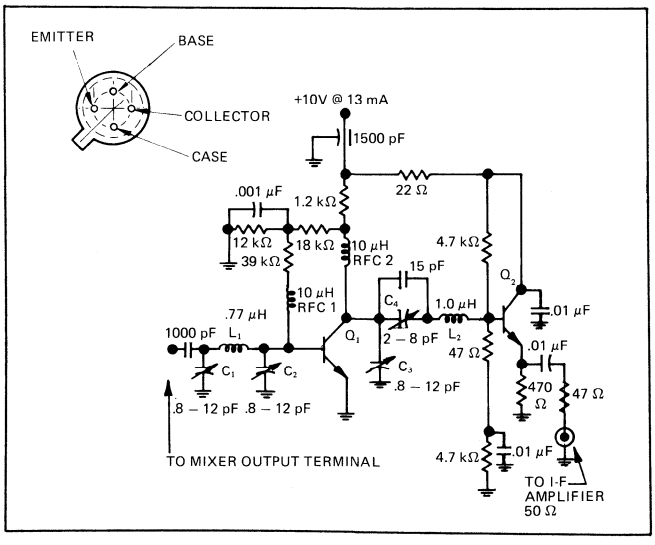
The particular devices selected for this application came from the MA-42000 series which are well suited for R.F. and I.F. amplifier applications up to 700 MHz. The MA-42001 was chosen for the first stage due to its excellent N.F. and wide dynamic range characteristics. A slightly higher N.F.-type device from the same series is used in the emitter-follower portion of the circuit, where noise figure is not of prime importance. A printed circuit board layout simplifies the construction of this preamplifier as shown below. It is recommended this board be completely enclosed for environmental protection. In practice, this preamplifier is mounted as close to the Gunnplexer mixer output as possible to achieve maximum sensitivity. For further information on this application, write for the Microwave Associates' brochure entitled "Solid-State Gunnplexer™ Transceiver for Amateur Communication Systems". The system described is similar to motion detection equipment which find application in distance measurements, speed measurements, direction monitoring and intrusion alarms. The brochure entitled "Microwave Components for Motion Detection" contains complete technical details of products serving this market segment.

30 MHz Low Noise I-F Preamplifier (Schematic)

C_1, C_2, C_3 – VC22G .8 – 12 pF or equivalent
C_4 – Erie Ceramic Trimmer 2 – 8 pF or equivalent
CR_1 – 1N4004 Silicon Diode or equivalent.
L_1 – 17 turns of #28 wire wound on a T-25-6 powdered iron toroid
L_2 – 20 turns of #28 wire wound on a T-25-6 powdered iron toroid
Q_1 – MA-42001-509 NPN Silicon Transistor, Microwave Associates, Inc.
Q_2 – MA-42003-509 NPN Silicon Transistor, Microwave Associates, Inc.
RFC_1, RFC_2 – 20 turns of #28 wire wound on a FT-230-06 Ferrite

Performance Data @ 30 MHz
Noise Figure = 1.1 dB
Gain = 19 dB
Bandwidth (–3 dB) = 10 MHz
Pout @ 1 dB Compression = –7 dBm





amplifier design examples

435 MHz AMPLIFIER

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INTRODUCTION

The "art" involved in the design of high frequency amplifiers is rapidly diminishing due to the utilization of S-parameters and computer optimization techniques. Now, an engineer may design a multi-stage high frequency amplifier with the aid of a computer in a few hours and be highly confident of the predicted results.

The 435 MHz low noise amplifier illustrated below is a good example of the employment of the combination of transistor data, engineering judgment, and computer optimization.

DESIGN APPROACH

Currently, Microwave Associates and other manufacturers of transistors intended for VHF, UHF, and microwave applications utilize S-parameters to describe the performance of their high frequency transistors. This fact alone attests to the usefulness of this parameter set in the design of high frequency amplifiers. In order to design transistor amplifiers, one needs S-parameters data, specific noise figure and bias point data, a computer analysis and optimization program, and sound engineering judgment.

The design example used to illustrate these points is a low noise 435 MHz amplifier intended for the reception of the down link communications channel of the OSCAR VIII satellite.

The design goals are: Noise figure 2 dB max, Gain 15 dB min, output VSWR 1.25 max, frequency 435 MHz.

Basically, the design approach is as follows:

1. Selection of the appropriate transistor.
2. Determination of the terminal impedances (both input and output) required to obtain the specific performance objectives.
3. Choice of appropriate network to present the desired terminal impedances.
4. Computer optimization of network component values.
5. Stability analysis over a broad band of frequencies.

TRANSISTOR SELECTION

The main criteria in selection of a transistor for this application is low noise figure with suitable gain. The intended device should also be completely specified and characterized in terms of S-parameters and noise figure data. Without such data, extensive analysis of the amplifier circuit is impossible unless, of course, the designer is willing to perform the transistor evaluation and characterization himself.

The Microwave Associates 42140 series of high frequency transistors is ideally suited for this application. The devices are completely specified and characterized over a broad range of frequencies. At optimum bias, i.e., the D.C. operating point which results in minimum noise figure, the MA-42141 has the following characteristics:

$s_{11} = 0.64 \quad @ \quad -112°)$ $\quad V_{CE} = 10V$

$s_{21} = 7.7 \quad @ \quad +111°)$ $\quad I_C = 5\ mA$

$s_{12} = 0.046 \quad @ \quad +41°)$ $\quad F = 435\ MHz$

$s_{22} = 0.72 \quad @ \quad -35°)$

$\Gamma os = 0.32 \quad @ \quad +38°$

$F_{min} = 1.80\ dB$

where Γos is the source reflection coefficient required for minimum noise figure.

TRANSFORMATION NETWORKS

Using this data, the design task is to synthesize the networks which present Γos to the input of the transistor while simultaneously presenting a complex conjugate match at the output of the transistor. If low noise figure was not the prime objective, the design task would be to synthesize the input and output networks which would simultaneously provide the complex conjugate impedances to the input and output of the transistor. These conditions would result in maximum gain but not lowest noise figure.

The initial use of the computer is in determining the complex conjugate of the output impedance. The computer performs this calculation through a program which solves the equation:

$$\Gamma_L = S_{22} + \frac{S_{22}\, S_{12}\, \Gamma_{os}}{1 - S_{11}\, \Gamma_{os}}$$

Also of interest is the input impedance of the network:

$$\Gamma_{in} \quad S_{11} + \frac{S_{21}\, S_{12}\, \Gamma_L^*}{1 - S_{22}\, \Gamma_L^*}$$

The asterisk designates the complex conjugate.

amplifier design examples

435 MHz AMPLIFIER

AMPLIFIER BLOCK DIAGRAM

The design tasks can be more easily understood through a study of Figure 1 which displays, in a block diagram form, a cascade of the input network, the transistor, and the output network. Figure 2 displays a Smith chart showing the locations of the various impedance points. The Smith chart will aid in the synthesis of the transforming networks

Figures 3 and 4 may now be used to determine the "ball-park" values for the transformation networks. Variable capacitors have been employed at the input to allow for the normal manufacturing variations as well as to extract the absolute minimum noise figure available from the transistor. A single variable capacitor is employed at the output to peak the gain and to minimize the output impedance match. For this application, variable capacitors are recommended since operation from and into ideal 50Ω

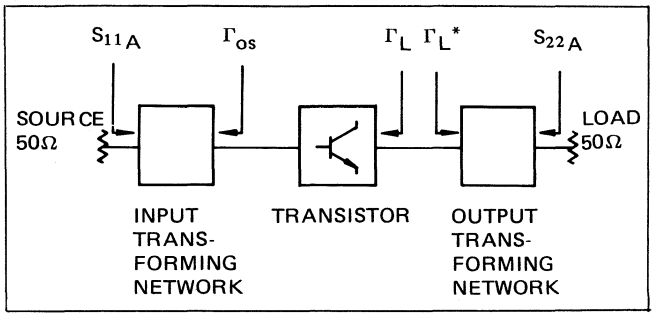

FIGURE 1. BLOCK DIAGRAM OF INPUT AND OUTPUT TRANSFORMAING NETWORKS

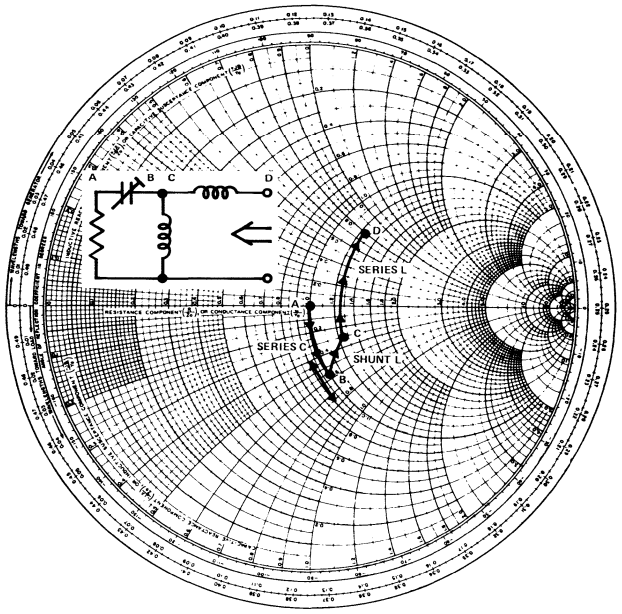

FIGURE 3. APPROXIMATE OUTPUT IMPEDANCE MATCH SHOWN ON SMITH CHART

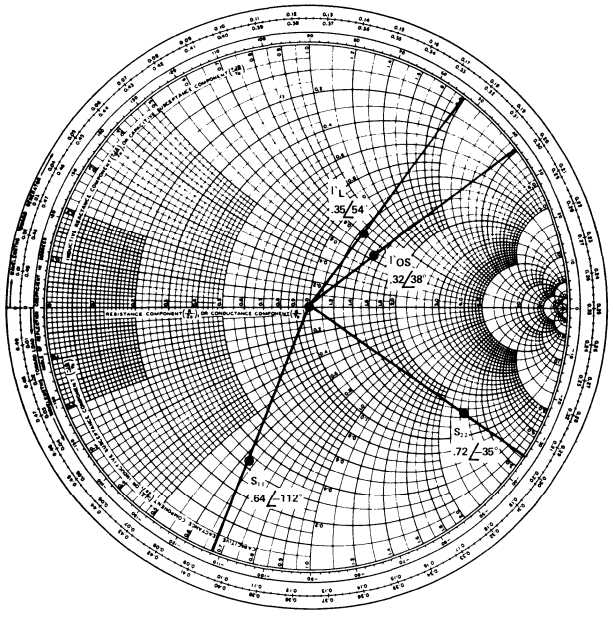

FIGURE 2. MATCHING PROBLEM DEFINED ON SMITH CHART

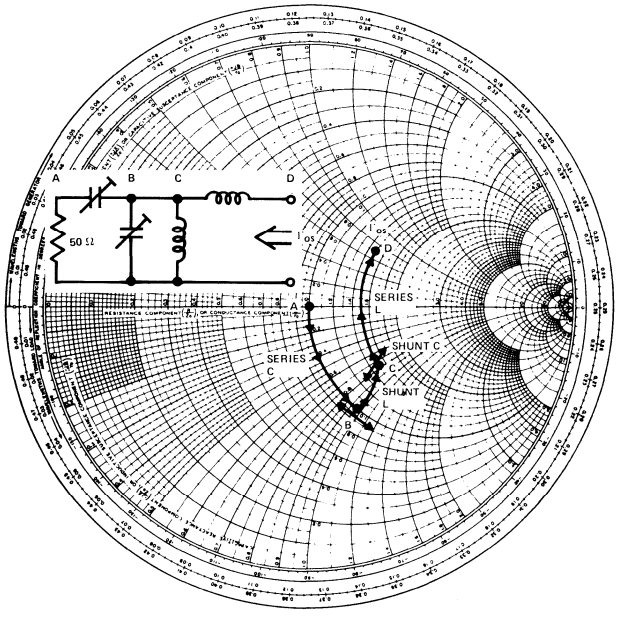

FIGURE 4. APPROXIMATE INPUT IMPEDANCE SHOWN ON SMITH CHART

amplifier design examples

435 MHz AMPLIFIER

NOTE: A 150Ω resistor is added, shunting the output of the transistor. This resistor was included to provide a margin of stability to the amplifier since the initial analysis in determining the complex conjugate of the output impedance indicated that the transistor was potentially unstable when terminated with these impedances. With the aid of the Smith chart plots of Figures 3 and 4, pg. 29, the networks required to transform the 50Ω source and load to the desired impedances may be designed. Smith charts are an indispensable tool in the design of impedance transforming networks which employ reactive circuit elements and transmission lines. Reference 4 will provide a clear understanding of Smith charts and their applications.

The calculations of approximate element values for the input and output networks is shown below. Figure 5 is a preliminary schematic of the amplifier. The elements below are defined in Figure 5.

INPUT ELEMENTS

$C_1 = \frac{1}{2\pi F X_{C_1}} = 7.3\ pF \quad X_C = 50\Omega$

$C_2 = 5\ pF$

$L_1 = \frac{X_{L_1}}{2\pi F} = 37\ nH \quad X_{L_1} = 100\Omega^*$

$L_2 = \frac{X_{L_2}}{2\pi F} = 27\ nH \quad X_{L_2} = 75\Omega$

OUTPUT ELEMENTS

$C_3 = \frac{1}{2\pi F X_{C3}} = 12.18\ pF \quad X_{C^3} = 30\Omega$

$L_3 = \frac{X_{L_3}}{2\pi F} = 20\ nH \quad X_{L_3} = 55\Omega$

$L_4 = \frac{X_{L_4}}{2\pi F} = 74\ nH \quad X_{L_4} = 200\Omega$

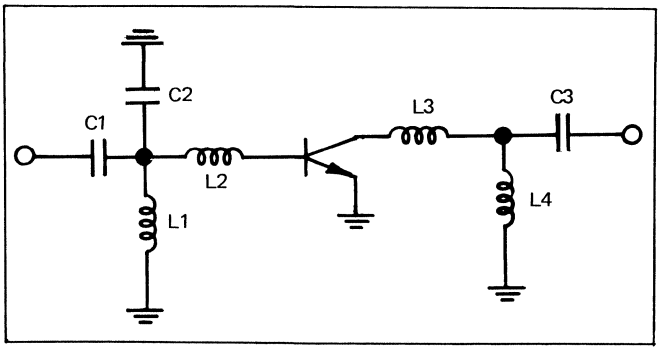

FIGURE 5. MATCHING NETWORK CHOSEN FOR DESIGN

*Parallel combination of L_1 and C_2 equals 250Ω of positive reactance.

NOTE: It is necessary only to determine a "ballpark" number for the elements since the computer program will adjust the values to optimize performance. However, values close to optimum will result in the usage of less computer time and, therefore, lower cost.

PRINTED CIRCUIT ELEMENTS

Rather than winding coils which could be lossy and cause stray coupling through unwanted radiation, it is possible to print lengths of line as inductive elements providing the line lengths are less than λ/8 and preferably less than λ/16. This is more easily seen if one examines the input impedance of a lossless short circuited transmission line,

$$Z_{IN} = +jZoTAN\left(\frac{2\pi\ell}{\lambda}\right) = +JZoTAN\ (\theta),$$

where,

- Z_{IN} = Input impedance of the transmission line
- Zo = Characteristic impedance of the transmission line
- ℓ = Length of the transmission line
- λ = Wavelength
- θ = Electrical length of the transmission line in degrees.

Note that this expression is a pure reactance which varies almost linearly with the electrical length θ, provided that θ is small. Therefore, by varying the characteristic impedance (Zo) and the electrical length (θ) one may synthesize inductance elements which are very accurate and highly repeatable with printed circuit techniques.

COMPUTER OPTIMIZATION

The next step in the design of the low noise amplifier is to select an appropriate computer program to execute the calculations and optimization. The COMPACT[1] Computer Program was used for this purpose because it possesses broad capability and is very modest in cost when used within certain guidelines.

The information for the computer is written in the form of a data file. Once the data file is written, the computer will vary the network elements, attempting to minimize the error between the desired circuit performance and the actual circuit performance. Specific performance parameters may be weighted such that their attainment carries more importance than other performance parameters. For example, if noise figure is the most important

1 COMPACT is an acronym for computer optimization of microwave passive and active circuits. Additional information is available by writing to: Compact Engineering, Inc., 1651 Jolly Court, Los Altos, CA 94022.

design goal, one may sacrifice input impedance match or gain so that the lowest noise figure may be achieved; the computer will adjust the variable elements in a direction which minimizes noise figure but not necessarily maximizing gain or lowering input impedance mismatch.

The analysis and optimization was performed for a single frequency (435 MHz); additional or broader frequency analysis and optimization could be performed by altering the data file. The cost of computer optimization varies with the number of variables and frequencies.

The computer analysis predicted the following performance at 435 MHz.

Noise Figure 1.81 dB
Power Gain 16 dB
Output VSWR 1.22

The computer designed circuit parameters are shown in Figure 6. The noise figure might be somewhat optimistic since no allowance has been made for circuit losses associated with the variable capacitors and high input VSWR.

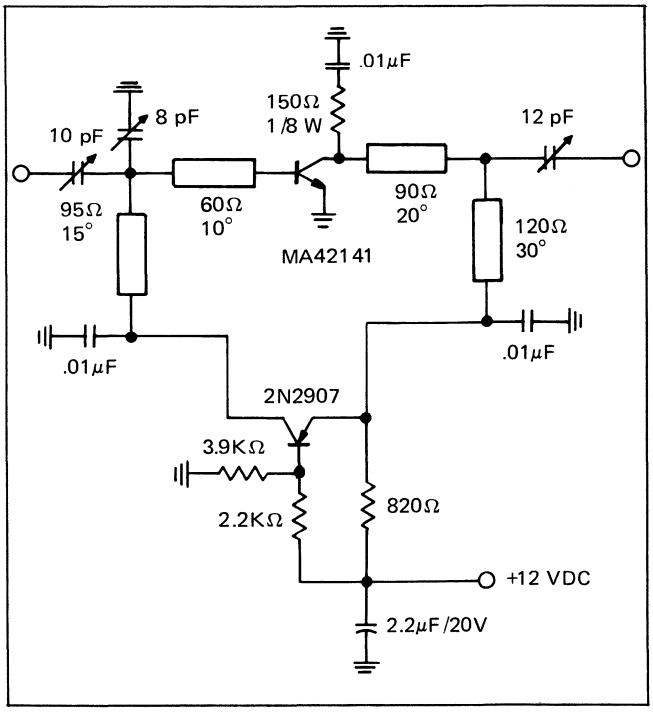

FIGURE 6. SCHEMATIC OF COMPLETE AMPLIFIER

TRANSISTOR BIASING CONSIDERATIONS

In order to realize the predicted performance, the designer must mount the transistor in a manner which closely approximates the electrical and mechanical environment under which the manufacturer obtained the data. The introduction of parasitic elements in mounting the transistor can lead to large discrepancies between the predicted and measured performance. The parasitic element which contributes most to performance degradation is the emitter lead inductance, which, if not kept to a minimum, will both reduce gain and alter the source impedance required for minimum noise figure. It may also introduce instabilities within the circuit which could result in oscillations. It is for these reasons that an active bias circuit will provide the proper collector to emitter voltage and collector current, while allowing a direct grounding of the emitter lead to minimize the introduction of any parasitic impedance into the circuit. A schematic diagram of the active bias circuit is shown in Figure 7. A brief description of the operation follows:

The active bias circuit is actually a feedback loop which senses the collector current of the RF transistor and adjusts the base current to hold that collector current fixed. The collector-to-emitter voltage of the RF transistor is held to a fixed potential determined by the voltage divider R_1 and R_2. The current through resistor, R_3, becomes the collector current of the RF transistor under the assumption (a good one) that the 2N2907 and the MA-42141 both have moderate D.C. Beta.

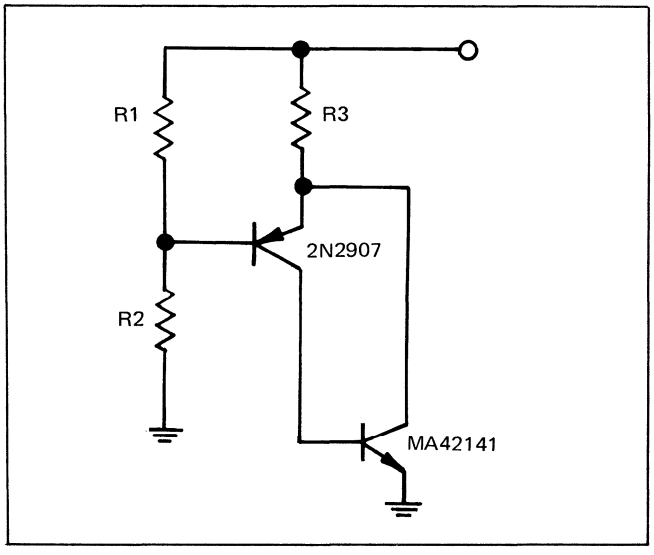

FIGURE 7. ACTIVE BIAS CIRCUIT

amplifier design examples

435 MHz AMPLIFIER

AMPLIFIER PERFORMANCE

A complete schematic diagram of the low noise amplifier is shown in Figure 7, pg. 31. The synthesized inductors are specified in terms of their characteristic impedance and electrical length. Figure 8 shows the photo mask used to make the microstrip circuit.

Table I below shows a comparison between the predicted and measured performance.

TABLE I

PERFORMANCE COMPARISON			
	Predicted	**Measured**	
		Unit #1	**Unit #2**
Noise Figure (dB)	1.8	1.9	1.9
Gain (dB)	16.1	16.0	16.5
Output VSWR	1.22:1	1.15:1	1.12:1

STABILITY CONSIDERATIONS

A broadband computer stability analysis reveals that the amplifier is unconditionally stable over a frequency band from 400 MHz to 2800 MHz. The importance of the stability analysis cannot be overemphasized for, in many applications, the source and load impedances may take on any value outside the particular frequency band of interest. When a high gain microwave transistor is used, it is most important to assure that the resulting amplifier does not oscillate as a result of various out of band source and load impedances.

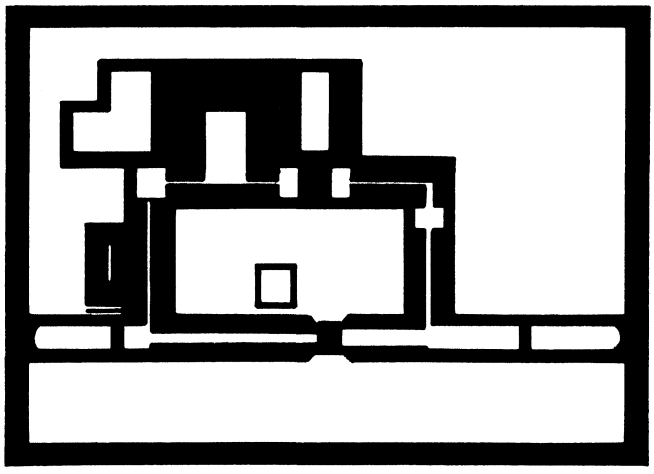

FIGURE 8. PHOTO MASK OF AMPLIFIER

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   (a) Philip H. Smith, Electronic Applications of the Smith Chart in Waveguide, Circuit, and Component Analysis, McGraw Hill, 1969

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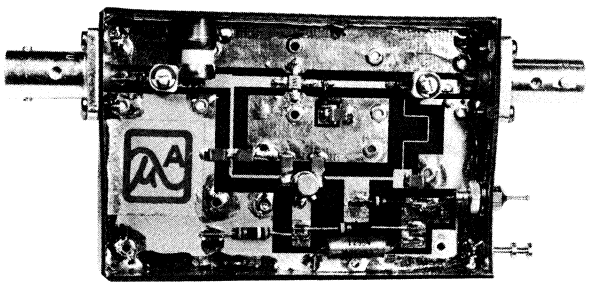
   (a) Scattering Parameters, Amplifier Design, pgs. 9-23.



amplifier design examples

2 GHz AMPLIFIER

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ABSTRACT

A 2.0 GHz amplifier is described. The single stage amplifier utilizes the MA-42161 biased at optimum noise figure. A computer aided design program was employed to optimize both input match and noise figure.

DISCUSSION

The schematic diagram of a 2.0 GHz low noise amplifier is shown in Figure 9. The amplifier is of planar microstrip construction on Teflon fiberglass circuit board (E_r = 3.55) and employs a MA-42161 transistor.

A computer analysis and optimization program (Compact) was used to analyze and optimize the circuit performance. On the finished circuit, the noise figure was measured to be 2.5 dB with an associated gain of 12 dB at 2.0 GHz.

In order to illustrate how parasitic elements such as emitter lead self inductance, effect the performance of such amplifiers, the program was used to analyze the same circuit without any emitter lead inductance. The analysis lead to a prediction of 2.6 dB NF with an input VSWR of 1.65:1 while the constructed unit had an NF of 3.1 dB with a 1.30:1 VSWR.

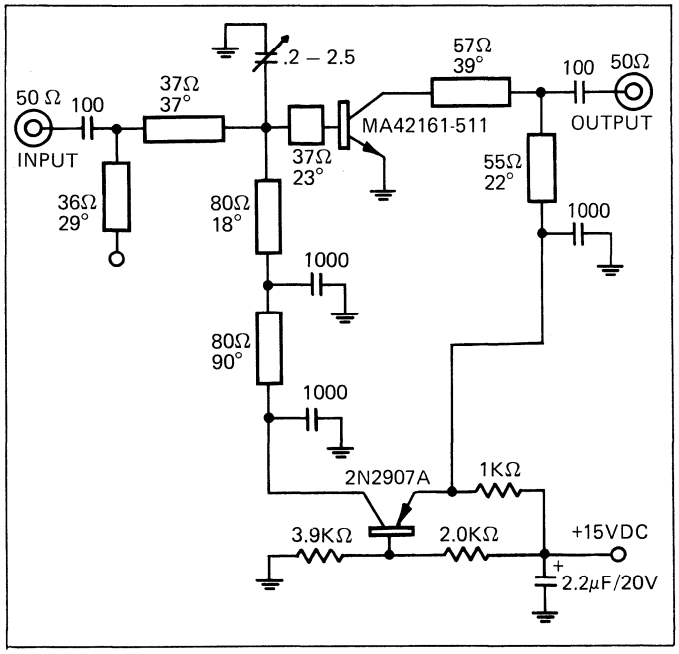
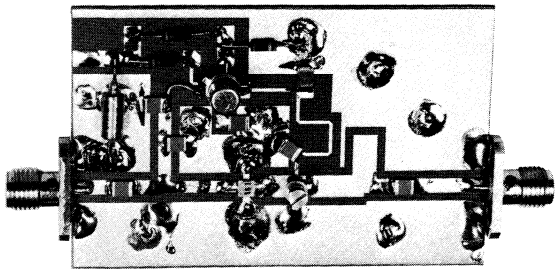
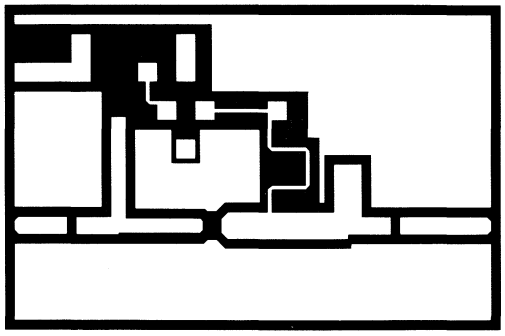


FIGURE 9. COMPLETE SCHEMATIC DIAGRAM OF 2-GHz AMPLIFIER. ALL CAPACITORS ARE IN PICOFARADS. RESISTORS ARE ¼ WATT.





THE CIRCUIT BOARD LAYOUT IS SHOWN ACTUAL SIZE. THE BOARD IS MADE .032 TGF, 1 OZ. COPPERCLAD BOTH SIDES.

oscillator design

OSCILLATORS

Most practical microwave transistor oscillators operate in a large signal mode, wherein, after build-up of the oscillations, the active device conditions determine the limits of signal swing (generally saturation and/or cut off). When the transistor is in this mode, any analysis of operations should be performed using large signal conditions. However, at initiation of oscillations and during build-up, the transistor is operating under small signal conditions allowing analysis to be performed using small signal parameters. In the past, most designs were done using small signal parameters (h, y, etc.) more suited to low frequency oscillators than to microwave oscillators. Now, the use of S-parameters in conjunction with powerful computer programs can aid the oscillator designer in determining an optimum circuit for his design. References 1 through 7 discuss this technique in detail.

The technique involves embedding the transistor in a circuit which will cause one port of the circuit to exhibit negative resistance.

To simplify the discussion relating negative resistance to oscillators and reflection coefficient, consider the one port negative resistance oscillator as shown in Figure 1.

The input admittance to the network is:

$$Y_{in} = G_n + j\omega\left(C + \frac{1}{\omega^2 L}\right) \qquad (1)$$

where G_n is a negative conductance. The circuit will oscillate if a load conductance is added whose conductance is less than $|G_n|$. The frequency of oscillation will be determined by the two reactive components.

Since the input admittance is negative, the corresponding input reflection coefficient (Equation 24) is greater than one. This represents an impedance point outside the $\Gamma' = 1$ circle of the Smith Chart.

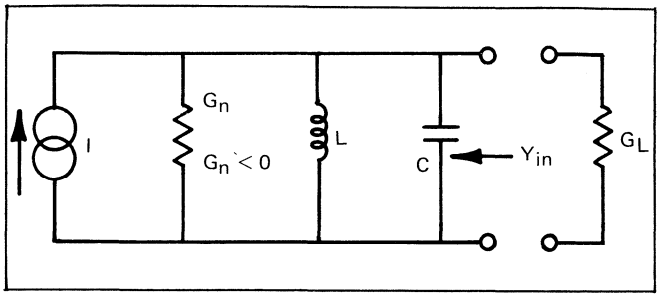


FIGURE 1. SIMPLE ONE PORT NEGATIVE RESISTANCE OSCILLATOR

Since the network is a one port, there is no decoupling between the tank circuit (L-C) and the load. This lack of decoupling may make it quite difficult to obtain significant amounts of power output without affecting the frequency of oscillation.

Adequate decoupling can be achieved if a two port device (a transistor) is used as the active element in the network. With the proper series or shunt feedback elements employed with the transistor, it is possible to have one port with a reflection coefficient greater than one. This port can then be loaded properly to sustain oscillations while power is coupled out from the remaining port. Figure 2 illustrates the use of a transistor as an active two port with a feedback impedance (Z_f) in the base circuit.

Network analysis computer programs[8] are available that can be used to determine the optimum circuit values for the tank circuit, feedback admittance and output matching network.

The first step in designing an oscillator is to select a transistor that with proper feedback, will exhibit a negative resistance to at least one port. The frequency of oscillation should be less than the selected transistor's f_{max} and the stability factor K should be less than one at the operating frequency. Generally, at microwave frequencies, the most effective transistor configuration for an oscillator is the common base configuration because it can supply higher gain and efficiencies at higher frequencies (frequencies above the transistor f_t) than the common emitter configuration. This configuration also has one port (input) with a large reflection coefficient.

If, for example, it was necessary to design a 2 GHz, 250 mW oscillator then the MA-42191-510 would be an ideal choice for design. Its maximum frequency of oscillation is 6.5 GHz and the stability factor is less than one at 2 GHz.

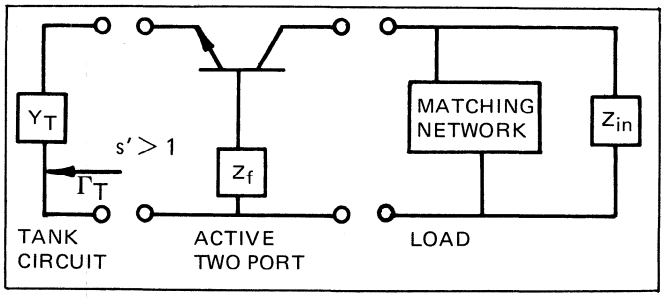


FIGURE 2. ACTIVE TWO PORT TRANSISTOR WITH FEEDBACK IMPEDANCE

The MA-42191-510 is supplied in the common base configuration. Referring to the MA-42190 series data sheet, it can be seen from the S-parameters at 2 GHz, that both the input and output impedances have negative real resistance components.

LOW POWER S-BAND OSCILLATOR

The MA-42151-511 transistor has been successfully employed in an S-band local oscillator for use in a 3.0 GHz Marine radar. The oscillator (Figure 3) was originally designed using empirical data, however, subsequent analysis was made using a computer circuit optimization program. This optimization procedure indicated that in order for the circuit to operate, a 5 nanohenry inductance must be in series with the base lead of this transistor. This inductance is in fact in the circuit and is due to the length of the base leads. This can be seen in the photograph of the oscillator below.

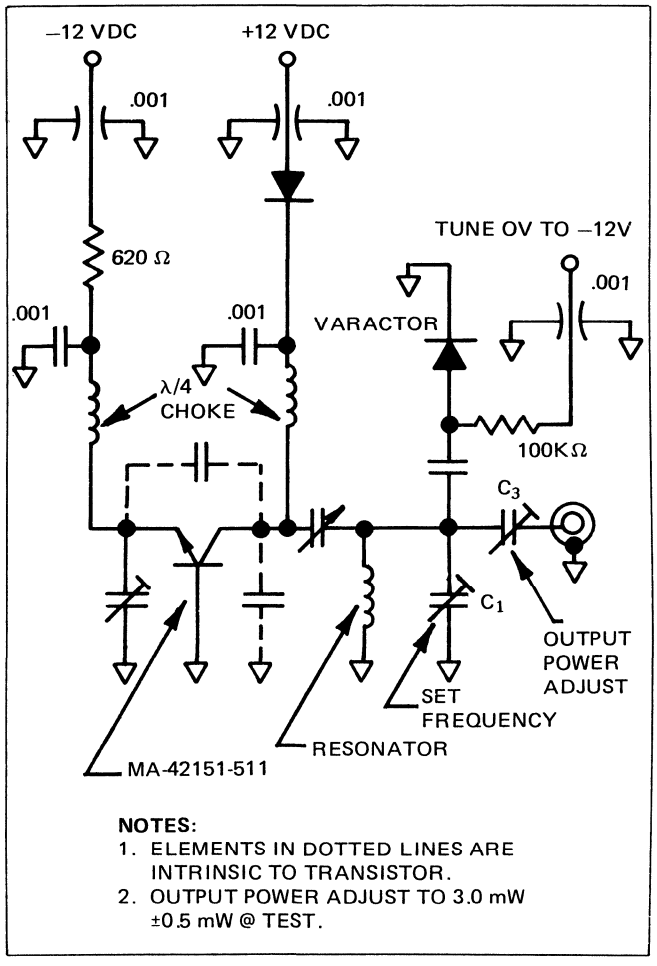


FIGURE 3. SCHEMATIC DIAGRAM, S-BAND OSCILLATOR

The oscillator can be mechanically tuned ±25 MHz using the capacitor, C_1, around 3.095 GHz. Remote electronic tuning is accomplished by biasing the varactor from 0 to −12 volts. The electronic tuning range is 8 MHz peak to peak. The power output is limited to 3.0 mW using C_3. The maximum power output is approximately 15 mW. The frequency temperature coefficient is −90 KHz/°C and all harmonics are greater than 25 dB down from the carrier. The pushing factor is in the 1.0 MHz/V range.

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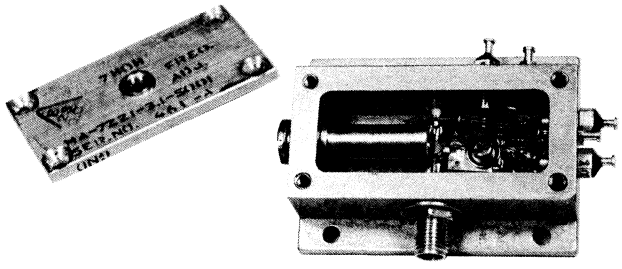

LOW POWER S-BAND OSCILLATOR

notes

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reliability

RELIABILITY: AN INTRODUCTION

Low-noise microwave transistors represent one of the pinnacles of the semiconductor art. Only the most technologically advanced companies are able to manufacture them and achieve the reliability levels demanded by today's system requirements. This reliability is obtained through a combination of extremely careful wafer processing, chip assembly and screening procedures.

Reliability is defined as the PROBABILITY of a device performing its purpose adequately for the period of time intended under the operating condition encountered. Notice that three things are needed to define reliability,

1) a probability of survival,
2) an operating time period,
3) and the operating conditions.

All three are expressed as precise numerical quantities and a statement of reliability that omits any one of the three conditions is of no value to the user. Thus, a statement that a part exhibits a failure rate of 10 FITS is meaningless unless the operating temperature and conditions are defined. (1 FIT is the failure rate if 1 failure occurs in 10^9 device hours of operation. A device hour can be obtained in any number of ways. It is one device operating for one hour or 2 devices operating for ½ hour, etc.)

For a single component series system, that is a system that fails if one component fails, a plot of system failure rate, as a function of time, will be identical to the component failure rate, as illustrated in Figure 1. This curve applies to

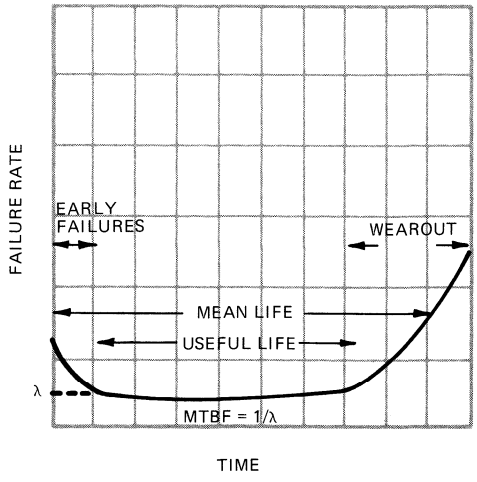

FIGURE 1. COMPONENT FAILURE RATE

any semiconductor device. Initially, the failure rate is higher than allowed by system design and is called the "early" failure period. These "early" failures are due to defects introduced in the manufacturing process which remain undetected despite the implementation of stringent processing controls.

The early failures are always brought to an acceptable level, before installation in any system, by electrical and environmental screening of finished devices, a process often referred to as "burn-in". After the initial early failure period, the system will settle down and exhibit a constant failure rate, λ.

The period during which the failure rate is constant is called the "useful life" of the system because it is in this period that the component can be utilized to the greatest advantage. The failures that do occur are called "chance failures". The physical mechanism of such failures is a sudden accumulation of stresses acting on and in the component. To minimize the chance failure rate, it is wise to operate components at specified rated levels which are conservatively chosen. Thus, if a device exhibiting a critical avalanche voltage of 20 volts is operated at 19.5 volts random system fluctuations are most likely to cause the critical avalanche voltage to be exceeded. It is much better to operate at 10 volts, in which case the chance failure rate due to this mechanism is reduced. Decisions about operating conditions are usually made jointly by the customer, who is attempting to achieve a required performance, and the device manufacturer who is aware of the limitations of his devices.

The reliability, R(t), at time, t, in the useful life region is given by:

$$R(t) = e^{-\lambda t} \qquad (1)$$

where the function R(t) is the probability that the device, which has a constant failure rate, λ, will not fail in the given operating time, t. The mean time between failures (MTBF) is merely the reciprocal of λ:

$$MTBF = \frac{1}{\lambda} \qquad (2)$$

Specifying MTBF is the most common way of expressing a parts reliability, but it must be used with caution. Before it can be applied to a particular situation, it is necessary to estimate the mean life of the component. The mean life is the time taken to fail half of a given population and includes failures from the wearout region. (See Figure 2, pg. 42.)

Wearout occurs at the end of a products' useful life and is a symptom of a components' aging. In most semiconductor circuit applications, the mean life is designed to be much greater than the intended life of the system so that wearout does not contribute to the failure rate.

To illustrate these concepts, consider purchasing one-hundred-thousand light bulbs. To establish an MTBF rating, each bulb could simultaneously be operated for 100 hours. Suppose 10 failed, the experimentally determined MTBF is:

$$MTBF = \frac{100{,}000 \times 100}{10} = 10^6 \text{ hours} \qquad (3)$$

which is a very impressive number. However, this does not mean that the bulbs can be operated 10^6 hours. Their mean life is probably several thousand hours and unless the user clearly understands the difference he may be disappointed after half a year to find out that only half the bulbs are still operational. MTBF estimates are of no value unless accompanied by an estimate of the parts' mean life.

Finally, if a component exhibited an MTBF of 10^6 hours, it means, using Equation (1), that the probability that the device will not fail in any given 10 hour period is 0.99999 or 99.999 percent, provided operation is restricted to the useful life period.

The major difference between the useful life period and the wearout region is that the failure rate, λ, is constant for chance failures, whereas it increases rapidly as wearout progresses and the operating time reaches the mean time. Much investigation of the wearout failure region has been performed with the result that characteristic failure mechanisms have been identified and in some cases reduced or eliminated. For example, the failure rate due to these mechanisms is a strong function of temperature and follows the Arrhenius law:

$$F.R. = Ae^{\frac{-Ea}{kT}} \qquad (4)$$

where

A = constant
Ea = activation energy
k = Boltzmann's Constant
T = temperature (°K)

At room temperature, for well designed and thoroughly screened parts, the mean life of semiconductor devices, whether it be microwave diodes or microwave bipolar transistors can exceed 10^8 hours (10,000 years). Experiments to study the wearout failure region at room temperature cannot be performed because of this time magnitude. However, if the temperature is raised sufficiently high enough, the failure rate will increase to a measurable level within a reasonable time-frame (100-10,000 hours). Such testing, called "Accelerated" or "Step-Stress" testing has been used to effectively assess the mean life of many semiconductor devices despite the implicit assumption that the failing mechanism(s) are the same at all temperatures. Experimental care and knowledgeable analyses are needed before such extrapolations can be made.

Activation energies have been assigned to various isolated failure mechanisms. These failure mechanisms have been determined by careful physical analysis of failed parts and three of particular importance to microwave transistors are given in Table I.

TABLE I

MECHANISM	Ea (eV)	REFERENCE
Oxide Charge Drift	~1.02	1
Electromigration		2
• Gold	~0.61	
• Aluminum	~0.48	
Gold Diffusion Through Titanium – Tungsten Refractory Metal Barrier	~1.8	1

Oxide charge drift, which leads to leakage current and low frequency parameter drifts was an early problem with most semiconductor devices. However, the rapid advances made in metal-oxide silicon (MOS) technology were brought about by the ability to control oxide charge drift through meticulous and clean processing schedules and today's microwave transistors fully utilize these technological advances. Seldom, if ever, do they experience this problem and wafers that do are removed internally through the use of screening procedures.

Because of the lower activation energy for aluminum electromigration compared to gold, it has been universally replaced by refractory gold metallization systems.

Finally, the very high activation energy of the gold refractory metallization system, where diffusion of gold finally penetrates the diffused junction, means that at normal system operating temperatures (<100°C) this mechanism does not contribute failures. As a consequence of these advances, for thoroughly screened Microwave Associates transistors operating at typical bias levels, the MTBF is in excess of 10^6 hours and the mean life (<100°C) will exceed 10^8 hours.

SEQUENTIAL SCREENING EXAMPLE FOR A HIGH-RELIABILITY TRANSISTOR

ENVIRONMENTAL RATINGS PER MIL STD 750

	Method	Level
Storage Temperature	1031	−65 to +200°C
Temperature Cycle	1051	10 cycles −65 to +200°C
Shock	2016	500 g's
Vibration	2056	15 g's
Constant Acceleration	2006	20,000 g's
Humidity	1021	10 days

***100% PROCESS CONDITIONING PER MIL STD 750**
2N2857 JAN/TX/TXV

Test	Method	Level
Internal Inspection	2072	
High Temperature Life (non operating, TX types only)	1031	Tstg = +200°C Time = 24 hours
Thermal Shock	1051	Test Condition C; 10 cycles; time at temperature extremes = 15 minutes minimum
Constant Acceleration	2006	20,000 G, in Y_1 orientation
Seal (leak rate)	1071	Fine Leak: Condition G or H maximum limit 1×10^{-7} Atm cc/sec. Gross Leak: Condition A, C, D, or F
High Temperature Reverse Bias	— — —	V_{CB} = 15V, I_E = 0, time = 48 hours, T_A = +150°C Limit: I_{CBO} = 10 nA maximum at conclusion of test

****100% POWER CONDITION PER MIL-STD-750**
2N2857 JAN/TX/TXV

Test	Method	Conditions
Pre-Burn In	— — —	Measure, Record I_{CES} and h_{FE}
Power Burn-In	— — —	V_{CB} + 15V, P_T = 200 mW, T_A = +25°C ±3°C, Time = 168 hours
Post Burn-In	— — —	ΔI_{CES} = +100% to −50% or 10 nA, whichever is greater Δh_{FE} = ±15%

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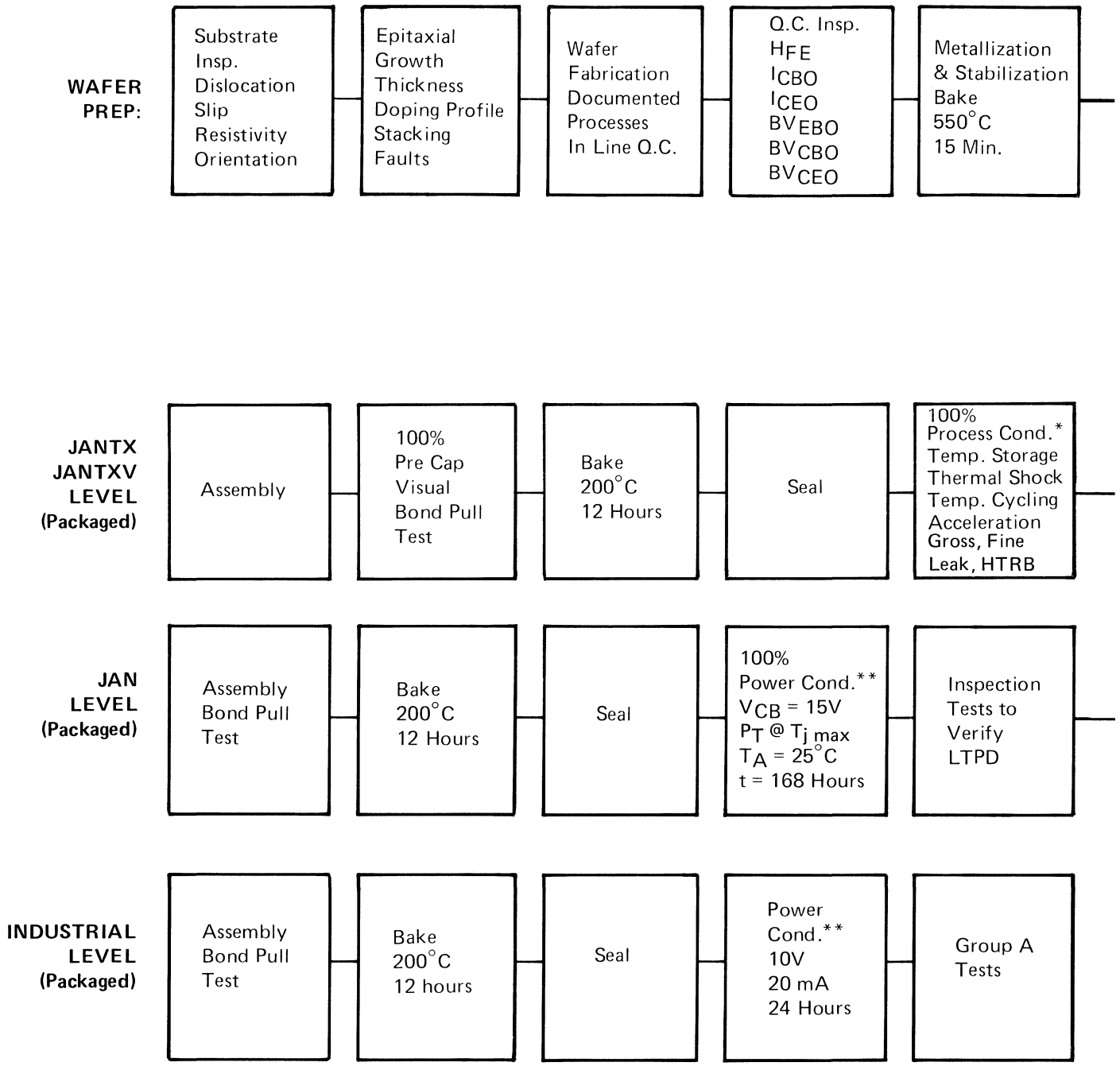
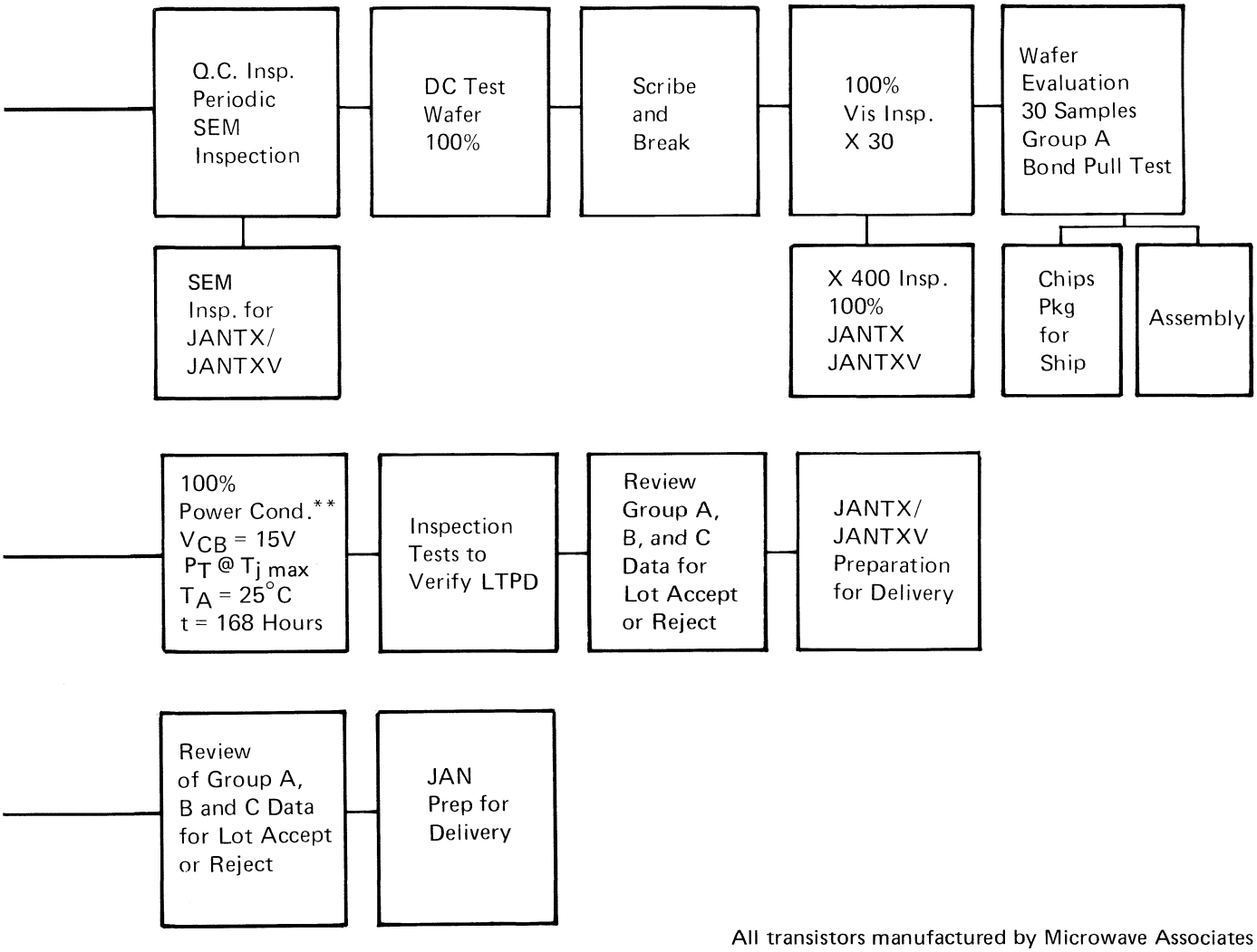


FIGURE 2. MICROWAVE ASSOCIATES PROCESSING SEQUENCES



All transistors manufactured by Microwave Associates have been designed to meet the environmental and screening requirements of MIL-STD-750, MIL-S-19500 and MIL-STD-883. They feature REFRACTORY METALLIZATION for ultra-reliable operation. Three standard levels are offered, JANTX/TXV, JAN and INDUSTRIAL. In addition, further screening levels can be accommodated as the customer desires, by contacting the factory. The processing sequences for each level from the initial wafer to final packaged unit is given in Figure 2.

Component screening to JAN and JANTX/TXV levels is designed to provide RELIABLE transistors suitable for military and space application. An introduction to general reliability concepts is included in this section.

* REFER TO PAGE 41
** REFER TO PAGE 41

glossary

A_i Current Gain
Current gain is the ratio of the output current to the input current. Current gain is also known as h_{fe} or Beta (β) for common emitter transistors, and as h_{fb} for common base transistors.

Current gain is a meaningful parameter for devices that have a very low input impedance (current sink) and a very high output impedance (current source). These conditions are met for low frequency operation and for some digital (switching) transistors.

Power gain is more important for most microwave applications than current gain.

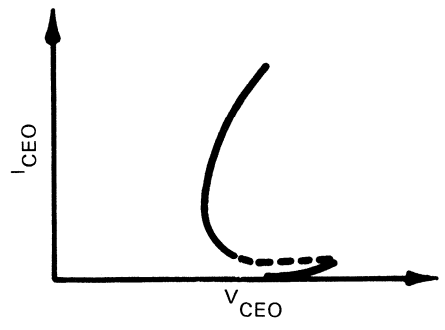
A_v Voltage Gain
Voltage gain is the ratio of the output voltage to the input voltage.

Voltage gain is meaningful for devices that have a very high input impedance and low output impedance. Then the output voltage of a device (such as a vacuum tube) is not loaded down by the low input impedance of the following stage.

Power gain is more important for most microwave applications than voltage gain.

BV Breakdown Voltage
Breakdown voltage is the reverse bias voltage at which a p-n junction begins to conduct a large current. The junction will not be damaged unless "excessive currents" are permitted to flow. What determines excessive current depends upon factors inherent in the design of the geometry. The magnitude of current flow can be restricted to a safe level by placing a suitable resistance in series with the power supply.

BV_{CBO} Collector Base Breakdown Voltage with Open Emitter
DC breakdown voltage, collector to base, with the emitter open circuited ($I_E = 0$). This is the highest breakdown voltage of the collector-base junction. BV_{CBO} is the highest voltage at which the transistor can be used without damage in Common Base circuits.



BV_{CEO} Collector Emitter Breakdown with Open Base
DC breakdown voltage, collector to emitter, with the base open circuited ($I_B = 0$). BV_{CEO} is usually lower (as much as 50%) than BV_{CBO}, and is an ususual function of current. See sketch. The dashed line represents a negative resistance region. BV_{CEO} is usually specified at the current corresponding to the minimum VC_{EO}.

BV_{CES} Collector Emitter Breakdown Voltage with Base Shorted
DC breakdown voltage, collector to emitter, with the base shorted to the emitter, ($V_{BE} = 0$). BV_{CES} usually has the same value as BV_{CBO}.

BV_{EBO} Emitter Base Breakdown Voltage
DC breakdown voltage, emitter to base reverse biased, with open circuited collector ($I_C = 0$). BV_{EBO} is of no consequence for small signal designs — its use is for (digital) switching circuits and occasionally for high power Class C amplifier design. Testing BV_{EBO} at currents greater than about 1 microamp can permanently damage the transistor, reducing h_{FE} and many gain parameters. For this reason the data sheets restrict BV_{EBO} to a maximum rating of 1.5 — 3.0 volts depending on the particular device.

CB Common Base
Common base refers to a transistor connected in a circuit so that the base is common to both input and output circuits (usually grounded). Common Base amplifiers have very low input impedances, making them difficult to be matched into a 50 Ω system. Thus, small signal amplifiers are rarely CB.

CB can result in negative input impedances, making this configuration desirable for oscillators. Common Base breakdown voltage is often higher than CE, so that some high power amplifiers are CB to allow safe operation at higher supply voltages.

CB biasing has the advantage of stability of the bias point versus changes in h_{FE} and temperature, making it highly suitable for test fixtures and production reproducibility of the bias point. It has the disadvantage of requiring two power supplies.

glossary

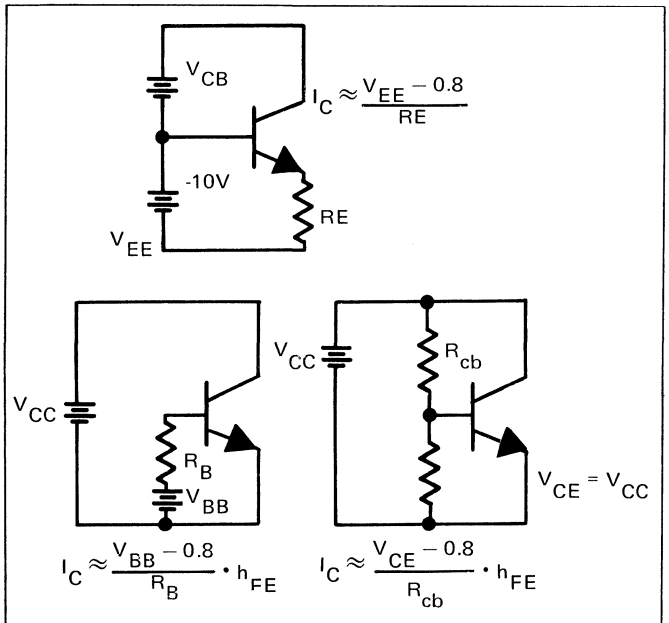
CC Common Collector
Common Collector refers to a transistor connected in a circuit so that the collector is common to both input and output circuits. CC was formerly popular for oscillators and for high power amplifiers before transistor packages with Beryllium-oxide insulated collectors were available.

An emitter follower is another name for a CC amplifier.

CE Common Emitter
Common emitter refers to a transistor connected in a circuit so that the emitter is common to both input and output circuits. The CE connection usually gives the highest power gain, but the real advantage is that the input impedance is closer to 50 Ω simplifying the designers impedance matching. Most small signal amplifiers are CE.

CE biasing has the advantage of not wasting bias (battery) power and requiring a single power supply voltage (economy). It has the disadvantage of poor bias point stability, with the collector current being a function of h_{fe} and V_{CC}.

To combine the advantages of CE and CB biasing, often feedback and/or active biasing networks are used for production circuits.



COMMON BIASING TECHNIQUES

Conjugate Match
A network port is said to be "conjugately matched" when connected to an impedance which, compared with the port impedance, has the same resistance and reactance, but the reactance has the opposite sign. Thus both reactances are "tuned" out between the port and the terminating impedance.

Maximum power transmission (i.e., no power reflected) is obtained only with a conjugate match. A conjugate match eliminates mismatch loss.

Cross-modulation
Cross-modulation Distortion (sometimes called XM or CM) is particularly undesirable because the modulation present on the undesired frequency is cross-modulated onto the carrier of the desired frequency.

Cross-modulation occurs when two (or more) signals are present in the input of an amplifier having a third order non-linearity:

$$e_{out} = k_1\ e_{in} + k_3\ (e_{in})^3$$

The amplitude of the cross-modulation distortion frequencies becomes increasingly large as either or both of the input signal levels are increased.

Cross-modulation distortion differs from inter-modulation distortion in that 1) modulation must be present on the undesired frequency and 2) the undesired frequency has NO frequency relationship to the fundamental.

A common occurence is that the modulation present on an adjacent frequency having high signal strength is cross-modulated into a weak desired frequency.

Dynamic Range
An important characteristic which summarizes the signal handling capability of the transistor in an amplifier. The limits are the 1-dB compression point (upper limit) and the noise figure (lower limit). Refer to the Amplifier Design Section for further details.

f_{max} Maximum Frequency of Oscillation
f_{max} is the theoretical frequency at which Maximum Available Gain equals unity (0 dB). f_{max} is an important figure of merit for microwave transistors, as it indicates the approximate upper frequency at which the transistor can be used as an oscillator. f_{max} is useful in approximating G_A (max).

f_{max} is difficult to determine for packaged transistors because G_A(max) versus frequency does not vary linearly as a function of 1/f due to package parasitics at frequencies approaching f_{max}.

f_s
Frequency where the forward transducer gain equals unity; $|S_{21}|^2 = 0$ dB.

f_t Transition Frequency ("Gain Bandwidth Product")
f_t is the theoretical frequency at which the common emitter current gain h_{fe} is unity (0 dB). It is of little direct value in designing microwave analog amplifiers, but is often included on data sheets for historical reasons. f_t is difficult to measure directly at microwave frequencies because of the difficulty in realizing a good microwave short circuit at the measurement plane of the transistor, without the transistor oscillating at some other frequency.

f_t is calculated from the common emitter current gain h_{fe} for several frequencies when h_{fe} varies linearly as 1/f. This line is extrapolated to the frequency f_t where h_{fe} is unity (0 dB). Device and package parasitics cause a deviation of the classic 1/f slope of h_{fe} as h_{fe} approaches unity.

f_t is sometimes referred to as the "Gain Bandwidth Product", which is misleading since the "gain" referred to is current gain. f_{max} could be referred to as the power gain bandwidth product.

Gain
"Gain" can mean power gain, voltage gain, current gain, or impedance gain. Unless otherwise specified, "gain" is assumed to be a power gain.

There are three types of power gain: Transducer Gain, "Power Gain", and Available Power Gain.

$$\text{"Power Gain"} \equiv \frac{\text{Power delivered to Load}}{\text{Power delivered to network input}}$$

$$\text{Available Power Gain} \equiv \frac{\text{Power Available at the Output}}{\text{Power Available from Source}}$$

$$\text{Transducer Power Gain} \equiv \frac{\text{Power Delivered to Load}}{\text{Power Available from Source}}$$

Of these three, Transducer Power Gain is by far the most commonly used.

G_A(max) Maximum Available Gain
G_A(max) is the theoretically highest transducer power gain that the transistor can deliver at a given frequency. Practical designs can approach G_A(max) within 0.5 to several dB, depending on the losses of the matching networks. It is important to recognize that G_A(max) is defined only for "stable" transistors (Stability factor "k" greater than 1.0). G_A(max) is defined for a simultaneous match for the input and output.

G_A(max) versus frequency has a slope of −6 dB per octave, approximately. f_{max} is the frequency where G_A (max) has decreased to unity (0 dB). Thus a convenient approximation for G_A(max) is:

$G_A(\max) = 20 \log\left(\frac{f_{max}}{f}\right)$ where f, the frequency at which the gain is being computed, is more than 0.1 f_{max} and less than 0.8 f_{max}.

The equation for G_A(max) in terms of S-parameters is somewhat formidable:

$$G_A(\max) = \frac{S_{21}}{S_{12}}\left(K \pm \sqrt{K^2 - 1}\right)$$

Where K is Rollett's stability factor, and the sign of the square root term is opposite that of B_1:

$$\text{where } B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |S_{11}S_{22} - S_{12}S_{21}|^2$$

GA Gain at Optimum Noise Figure
Noise Figure Gain is the transducer gain measured with the same source impedance as that used for obtaining Optimum Noise Figure (NF_O). This gain is usually a few dB lower than G_A (max) because the optimum source impedance for NF_O is usually different than that for G_A (max).

G_T Transducer Power Gain
G_T is the general transducer power gain. It is tedious to calculate without the aid of a computer because no assumptions are made about S_{12}, S_{11}, S_{22}, and Source and Load impedances.

Transducer power gain is meaningful because it is an insertion power gain, which is the way amplifiers are most commonly and easily tested.

$$G_T = \frac{|S_{21}|^2 \ (1 - |\Gamma_s|^2) \ (1 - |\Gamma_L|^2)}{\left|(1 - S_{11}\Gamma_s) \ (1 - S_{22}\Gamma_L) - S_{12}S_{22}\Gamma_L \ \Gamma_s\right|^2}$$

glossary

The maximum value of G_T for an unconditionally stable transistor is G_A (max).

G_{Tu} Unilateral Transducer Power Gain

Unilateral transducer power gain is the same as transducer power gain except that S_{12} is assumed equal to zero. This assumption is often justified, and simplifies the calculation of gain. When constant gain contours (circles) are plotted, they are associated with G_{Tu}.

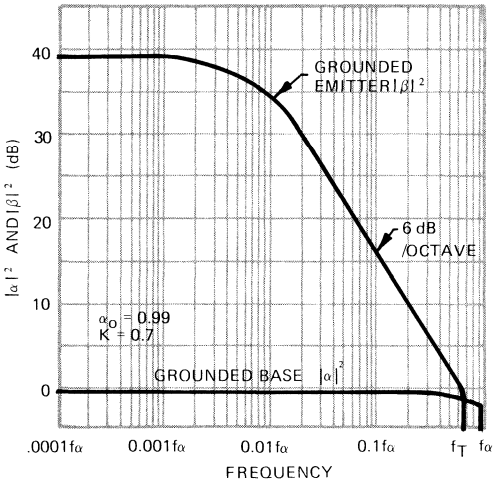
G_u(max) Maximum Unilateral Transducer Power Gain

G_u (max) is the highest transducer power gain the transistor can deliver when assumed unilateral (S12 = 0). The popularity of G_u (max) arises from its simplicity of calculation, and the fact that the unilateral assumption often results in only a negligible error in gain.

h_{fe} D.C. Forward Current Transfer Ratio, Common Emitter

Common Emitter Short Circuit AC Current Gain

h_{fe} is the small signal AC ratio of collector current to base current. Its response to change in frequency is shown below:



FREQUENCY DEPENDENCE OF $|\alpha|^2$ AND $|\beta|^2$

h_{FE} Common Emitter Current Gain, "Beta"

Common emitter DC current gain is the ratio of the total DC collector current to the total DC base current. h_{FE} is useful to the circuit designer in controlling the DC collector (Bias) current. Transistors of the same type from the same manufacturer often have a production spread of h_{FE} of 4 to 1, and specified limits of 10 to 1 are not unusual. Thus minimum typical and maximum limits of h_{FE} are needed by the designer.

h_{FE} is slightly smaller in magnitude than h_{fe} (or h_{feo}), especially at small collector current levels.

h_{feo} Low Frequency Common Emitter AC Current Gain

h_{feo} is the low frequency value of h_{fe}. h_{feo} can be easily measured with a transistor curve tracer. h_{feo} is often abbreviated as h_{fe}.

I_B(max) Absolute Maximum Base Current

I_B(max) is the largest base current that the transistor can safely withstand for an extended period of time. Exceeding I_B(max) can result in "metal migration" in the metallizing fingers, eventually open circuiting the base.

Greatly exceeding I_B(max) can result in instantaneously evaporating the base metallization.

I_{EBO} Emitter Base Leakage Current

DC leakage current, reversed biased emitter to base, with collector open (I_C = 0). I_{EBO} has no direct microwave design use other than its association with BV_{EBO}.

I_{CBO} Collector Base Leakage Current

DC leakage current, reversed biased collector to base, with emitter open circuited (I_E = 0). I_{CBO} is a measure of the reliability of the collector base junction. It is one of the more common screening parameters for high reliability. Excessive I_{CBO} can degrade s_{22} and h_{FE}, making biasing difficult.

I_{CEO} Collector Emitter Leakage Current with Open Base

DC leakage current, collector to emitter, with base open circuited (I_B = 0). For the same reverse bias I_{CEO} is usually larger than I_{CBO}.

To estimate whether I_{CEO} or I_{CBO} is the proper leakage current to use for a given circuit, determine the value of the DC resistance path between the emitter to base. If R_{EB} is

higher than several K-ohms, use I_{CEO}. If R_{EB} is less than about 100 ohms, use I_{CBO} or I_{CES}.

I_{CES} Collector Emitter Leakage Current Base Shorted

DC leakage current, reverse biased collector to emitter, with base shorted to emitter ($V_{BE} = 0$). I_{CES} has approximately the same magnitude as I_{CBO}, and is sometimes used as an alternative to I_{CBO} to eliminate the possibility of oscillations during high-speed automated testing.

I_C Absolute Maximum Collector Current

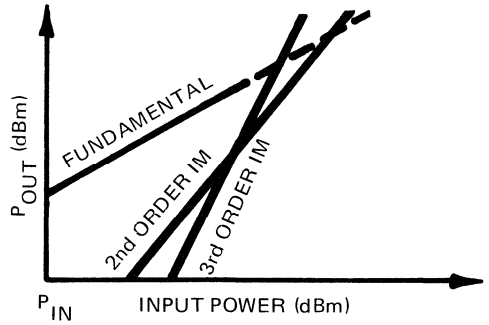
I_C (max) is the largest collector current that the transistor can safely withstand for an extended period of time.

Since most of the collector current flows through the emitter, excessive I_C (max) will generally damage the emitter metallization. High collector current flowing with high V_{CB} may induce damage from excessive power dissipation.

IM Distortion Intermodulation Distortion

Intermodulation distortion occurs when two (or more) signals of different frequency are applied to an amplifier which has a "non-linear transfer characteristic". The output signal spectrum contains, in addition to the input frequencies, other frequencies which are sums and differences of both 1) the input frequencies and 2) the harmonics and fundamentals of the input frequencies in all their combinations. The amplitude of the IM products increased two or three times as much as any input amplitude increase. All amplifiers will produce IM distortion if driven by a sufficiently large input signal.

IM is undesirable because new frequencies are created in the amplifier output which were not present in the input. There are two common forms of IM: Second Order IM and Third Order IM. No modulation is required to produce IM.



Intercept Point Second Order Intercept Point Third Order Intercept Point

The Intercept Point is a convenient method for specifying the Second Order or Third Order Harmonic Distortion of an amplifier. It is difficult to spec the Intercept Point of a transistor alone because the distortion is quite circuit dependent (Source, Load and Feedback impedance must be specified at the appropriate fundamental and harmonic frequencies). For further information, refer to the Amplifier Design application note.

K Rollett's Stability Factor

Stability Factor K is a figure of merit as to whether or not a transistor can oscillate for some combinations of source and load impedance. If K is larger than 1.0 then the transistor is "unconditionally stable". No source or load impedance will cause the transistor to oscillate at that frequency (except for negative resistance). If K is less than 1.0, oscillation is possible, and the transistor is "potentially unstable".

It is important to understand that the Stability Factor is very sensitive to feedback impedances in the emitter, base, or shunting the collector base. Also, to guarantee that oscillation will not occur at any frequency the stability factor would have to be checked at all frequencies from 0 to f_{max}.

$$K = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|}$$

Mason's Invariant

Mason's Invariant (Mason Gain, U) is the most unique figure of merit for a device. It is defined as the forward power gain in a feedback amplifier in which the reverse gain has been adjusted to zero by a lossless reciprocal feedback network. Because of the feedback loop employed in the measurement of the Mason invariant, the transistor may be imbedded in any lossless reciprocal network without changing the Mason invariant. This makes this gain parameter invariant with respect to any lossless header parasitics or changes in common lead configuration. Mason's Invariant is determined using the following expression:

$$U = \frac{1}{2}\left[\frac{|S_{21}/S_{12} - 1|^2}{K|S21/S12| - R_e\,(S21/S12)}\right]$$

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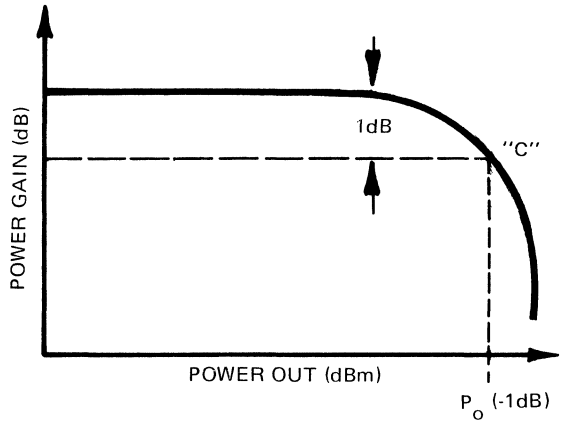
N.F. Noise Figure
The electrical noise characteristic of the transistor, usually expressed as the ratio of device noise to the thermal noise at 25°C. This ratio is generally in terms of decibels. Refer to the Amplifier Design application note.

NF_{opt} Optimum Noise Figure
Optimum Noise Figure is the lowest NF that the transistor can produce under the most favorable conditions of source and load impedance and bias at a specified frequency.

P_{out} Output Power
The microwave output power level delivered from a transistor to a load is P_{out}. Appropriate units for P_{out} are millwatts (mW), watts (W), and dBm (power in dB referenced to 1.0 millwatt).

P_{out} at 1 dB Gain Compression
When input power is increased, the output power will increase in a linear fashion until further increases of input power no longer produces a proportional increase in output power. The point where further increases in input power cause the output power to decrease 1 dB from the linear portion of the curve is called the 1 dB compression point. This can be expressed graphically as shown. The output power at point "c" corresponds to the 1 dB gain compression output power. This is a useful comparative measure of the maximum output capability of a linear amplifier, though distortion may be high. For further details, refer to the Amplifier Design Application notes.



P_T Total Power Dissipation
The total Power Dissipation is the sum of the DC and microwave power the transistor must dissipate.

$$P_T = (V_{CE} \times I_E) + [\text{Microwave Power } (P_{in} - P_{out})]$$

P_T is a function of case or ambient temperature, as graphed on the Power Temperature derating curve. The microwave power is negligible for small signal applications. Excessive power dissipation will result in excessive temperature of the collector base junction, and failure of the transistor.

P_T(max) Maximum Power Dissipation
P_T(max) is the maximum total DC and microwave power dissipation the transistor chip and package combination can safely withstand. This is a steady state rating unless otherwise specified. P_T(max) is reduced when the case or ambient temperatures exceed the corner temperature on the Power-Temperature derating curve.

Γ Reflection Coefficients
Reflection Coefficient is a measure of how close an impedance is to the characteristic impedance (e.g., 50 ohms). The reflection coefficient is a polar representation of impedance on the Smith Chart. Reflection coefficient is directly related to impedance and to VSWR. In a 50 ohm system,

$$\Gamma = \frac{Z - 50 \text{ ohms}}{Z + 50 \text{ ohms}} \quad \text{and} \quad \Gamma = \frac{VSWR - 1}{VSWR + 1}$$

Γ_L Load Reflection Coefficient
The load impedance reflection coefficient is, like Γ_S, used as an alternative expression for load impedance Z_L.

Γ_S Source Reflection Coefficient
The source impedance reflection coefficient is often used as an alternative expression for source impedance Z_S. Γ_S mathmetically simplifies many S-parameter equations and is easier to plot on the Smith Chart than Z_S.

$$\Gamma_S = \frac{Z_S - 50}{Z_S + 50}$$

$\Gamma_{s\ opt}$ Source Reflection Coefficient for Optimum Noise Figure

$$\Gamma_{s\ opt} = \frac{Z_{s\ opt} - Z_o}{Z_{s\ opt} + Z_o} = \frac{Z_{s\ opt} - 50\ ohms}{Z_{s\ opt} + 50\ ohms}$$

T_A Ambient Temperature

The Ambient Temperature is the temperature of the air surrounding the transistor. T_A is associated with packaged transistors which are not physically heat sunk with a stud, bar, or other mechanical contact, where the appropriate thermal resistance path is from the collector base junction to the air.

T_C Operating Case Temperature

The Operating Case Temperature is the temperature of that part of the transistor package which is attached to a heat sink.

T_C is the temperature of the heat sink itself if the heat sink is a good thermal conductor, and the heat sink temperature is measured adjacent to the transistor package.

Case Temperature is often assumed the same as ambient temperature T_A when the thermal resistance of the heat sink to ambient is negligible compared with the thermal resistance from junction to case θ_{JA}.

T_J(max) Maximum Junction Temperature

The maximum junction temperature is the maximum temperature at which the reverse-biased collector base junction can be maintained without irreversibly damaging the transistor. T_J(max) is often lower than T_{STG} because of the reverse bias voltage present in T_J(max).

T_{STG} Storage Temperature

The storage temperature is the maximum and minimum temperatures at which the transistor can be stored for an indefinite period of time with no bias applied without damage to the transistor. Damage from temperatures below the minimum recommended can result from thermally induced mechanical stress. Damage from temperatures above the maximum recommended can result from irreversible chemical changes in the transistor.

θJA and θJC Thermal Resistance Junction to Ambient Thermal Resistance Junction to Case

Junction to ambient thermal resistance is the inverse of the slope of the power dissipation derating curve. The smaller the value of θ_{JA} or θ_{JC} the steeper the slope of the derating curve. The smaller the thermal resistance, the less temperature drop from junction to case or ambient required to dissipate the internally generated power.

Whether to use θ_{JA} or θ_{JC} depends on how most of the thermal energy (heat) flows from the package. When the heat is removed by radiation and convection to the air, the θ_{JA} is the appropriate thermal resistance. When the heat is removed primarily by conduction, as through a stud or bar, then θ_{JC} is appropriate. The expression for junction temperature is:

$$T_J = T_A + \theta_{JA} \cdot P_T$$

S-Parameters

"S" Parameters are transmission and reflection coefficients utilized by VHF, UHF and microwave designers. All of the S-Parameters are analogous to the "h", "y", and "z" parameters. Transmission coefficients may be a gain or an attenuation characteristic, and reflection coefficients relate to VSWR and impedance. Refer to the S-Parameter discussion in the Amplifier Design Section.

s_{11} Input Reflection Coefficient

$$|s_{11}|^2 = \frac{\text{Power reflected from the transistor input}}{\text{Power incident on the transistor input}}$$

s_{11} can be considered as being related to the transistor input impedance. When the magnitude of s_{11} is greater than 1.0, the transistor has a negative input impedance, which is desirable for an oscillator.

s_{22} Output Reflection Coefficient

$$|s_{22}|^2 = \frac{\text{Power reflected from the transistor output}}{\text{Power incident on the transistor output}}$$

s_{22} can be considered as being related to the transistor output impedance. s_{22} is measured with the transistor input terminated with 50 Ω.

glossary

s_{21} Forward Transmission Coefficient

$$|s_{21}|^2 = \frac{\text{Power delivered to a 50 ohm load from the transistor}}{\text{Power available from a 50 ohm source}}$$

$|s_{21}|^2$ is the forward transducer power gain with a 50 ohm source and load for the transistor. s_{21} is the square root of the 50 ohm forward power gain.

s_{12} Reverse Transmission Coefficient

$|s_{12}|^2$ = Reverse transducer power gain with 50 ohm source and load. It is desirable that s_{12} be small. If s_{12} is large, the transistor has an increased tendency to oscillate. If s_{12} is large, the input impedance is affected strongly by the output impedance, and vice versa: Circuit design becomes more difficult.

V_{CE} (Sat)

Voltage between the collector and emitter terminals when the transistor is being operated in the saturation region of its operating characteristic.

VSWR Voltage Standing Wave Ratio

When a transmission line is terminated in some impedance other than Z_O, standing waves are produced from the combination of reflected power with the incident power. The ratio of the peak to valley of this standing wave is the voltage standing wave ratio (VSWR). VSWR is not a complex number. VSWR is easily related to the magnitude of an impedance but not relatable to its phase angle.

$$\text{VSWR} = \frac{Z}{Z_O} \text{ if } Z > Z_O \qquad \text{VSWR} = \frac{Z_O}{Z} \text{ if } Z < Z_O$$

Examples for a 50 ohm characteristic impedance:

Impedance	Reflection Coefficient	VSWR	Comments
R + jX	ρ or Γ	γ	Resistive Ohms + j Reactive Ohms
50 + j0	$0.0\angle 0^\circ$	1.0	Termination in characteristic impedance
0 + j0	$1.0\angle 180^\circ$	∞	Short Circuit
$\infty + j\infty$	$1.0\angle 0^\circ$	∞	Open Circuit
75 + j0	$0.2\angle 0^\circ$	1.5	75 ohm termination
50 + j50	$.45\angle +63^\circ$	2.6	Arbitrary complex load
50 − j50	$.45\angle -63^\circ$	2.6	Arbitrary complex load

Z_L Load Impedance

The load impedance Z_L is the impedance seen by the transistor output terminals (output port). Z_L is NOT the transistor output impedance.

Load impedance is important because power gain, output power level, and overall amplifier VSWR are functions of Z_L.

Z_O Characteristic Impedance

The characteristic impedance of a transmission line is the impedance seen looking into an infinite length of that transmission line. For most systems, the characteristic impedances are 75 ohms for CATV, 600 ohms for the telephone industry, and 300 ohms for television twin-lead transmission line. Characteristic impedance is purely resistive except for lossy lines.

$$Z_O = \frac{R + jwL}{G + jwC}$$

Where R, L, G, and C are per unit length of the transmission line.

Z_s Source Impedance

The source impedance is the impedance seen by the transistor input terminals (port). The reference plane is at the edge of the transistor package, perpendicular to the input lead. Z_S is NOT the transistor input impedance.

Source impedance is important because power gain, noise figure, and overall amplifier VSWR are functions of Z_S.

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Application	Model Number	Frequency Range (MHz)	Max. Noise Figure (dB)	Max. Gain (dB)	1-dB Compression @ Opt. N.F. (dBm)	Test Frequency (MHz)	F_T (GHz)	Standard Package	Page
Low Noise General Purpose R.F. Amplifiers	MA-42001	10-700	1.0	27	0	60	2.0	509, 510, 511, 520	59
	MA-42025	10-700	2.5	13	–10	450	1.8	509, 520	67
	MA-42051	200-1000	2.2	15	–10	450	2.5	509, 510, 511, 520	71
	MA-42111	60-2000	1.5	19	0	450	4.5	509, 510, 511, 520	77
	MA-42123	10-1000	2.3	13	–10	450	1.5	509, 520	83
	MA-42141	200-2000	2.5	16	0	1000	4.0	509, 510, 511, 520	89
	MA-42161	500-4000	2.5	14	– 5	2000	8.0	511, 512, 520	99
	2N2857 JAN TX/TXV	10-700	4.5	21	–10	450	1.8	509, 520	113
	2N6665	10-700	1.0	27	0	60	2.0	509, 520	121
Wide Dynamic Range Amplifiers	MA-42005	10-700	2.0	30	+19	60	2.0	509, 520	59
	MA-42010	10-700	3.5	20	+22	450	2.0	510, 520	59
	MA-42181	10-2000	5.0	14.5	+25	1000	2.9	510, 520	103

Application	Model Number	Frequency Range	Power Output	Input Power (DC)	Test Freq. (MHz)	F Max. (GHz)	Standard Package	Page
Low, Medium Power Oscillators	MA-42151	400 MHz - 3.0 GHz	25 mW	200 mW	3000	9.0	511, 520	95
	MA-42121	10 MHz - 1.5 GHz	50 mW	300 mW	1500	4.2	508, 520	67
	MA-42191	10 MHz - 3.0 GHz	350 mW	1.0 W	2000	6.5	510, 520	107

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KMC PRODUCT AVAILABILITY AND EQUIVALENT MA P/N

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KMC P/N	MA P/N
2069	42020
2070	42023
2071	42021
2072	42024
2073	42028
2112	42025
2113	42026
2114	42027
2115	42029
2116	42020
2117	42021
2118	42022
5201	42141
5204	42142
5510	42143
5525	42142
5526	42056
5527	42142
6001	42001
6001N	42014
6002	42002
6003	42003
6007	42111
6008	42008
6009	42009
6011	42004
6012	42005
6015	42006
6021	42010
6022	42011
6061	42015
6062	42016
6063	42012

JEDEC TRANSISTORS

2N2857
2N2857 JAN
2N2857 JAN TX
2N2857 JAN TXV
2N3570
2N3571
2N3572
2N3683
2N3839
2N3880
2N3953
2N5031
2N5032
2N5053
2N5054
2N5179
2N5651
2N5652
2N6618
2N6665

Contact manufacturer for availability of KMC Transistors not included in this list.

TRANSISTOR PACKAGE CROSS REFERENCE

KMC	MA	JEDEC
K	509	TO-72
KB	514	TO-50
KD	510	— — —
KF	506	TO-5, TO-39
KJ	511	— — —
KK	512	— — —
KX	508	TO-46

KMC package style is designated by a letter-type prefix. (i.e. K2069)
MA package style is designated by a number-type suffix. (i.e. MA-42020-509)

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specification sheets

specification sheet

npn silicon planar transistors

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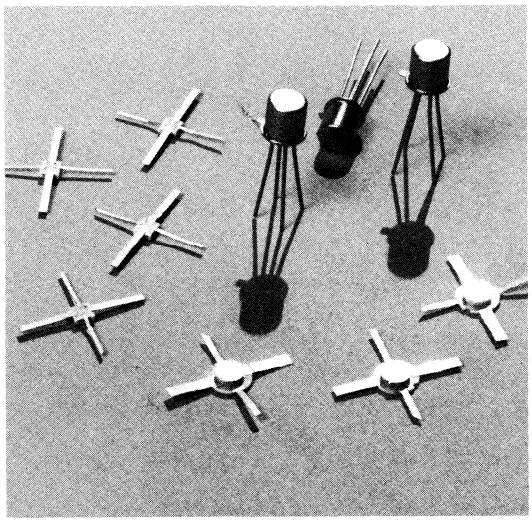
FEATURES

- LOW NOISE FIGURE (.8dB TYPICAL @ 60 MHz)
- LARGE DYNAMIC RANGE (+25dBm @ 1dB COMPRESSION POINT)
- GOLD METALLIZATION
- LOW COST
- HIGH RELIABILITY
- LOW 1/f NOISE (1.0 dB TYPICAL @ 10 KHz)

DESCRIPTION

This series of npn silicon planar transistors is designed to provide the lowest possible noise figure at frequencies from 10 to 700 MHz. These transistors exhibit excellent noise figure vs. current characteristics which results in extremely low noise and wide dynamic range performance. These transistors find wide application in sophisticated radar and communications equipment at VHF/UHF.



APPLICATIONS

IF, VHF, UHF, TV and RF Amplifiers.

MA-42000 SERIES R.F. SPECIFICATIONS (Case Temperature 25°C)

MODEL NO.	MA-42001	MA-42014	MA-42002	MA-42003	MA-42004	MA-42005	MA-42006	MA-42008
CASE STYLE[1]	509	509	509	509	509	509	510	511
KMC Model No.[4]	K6001	K6001N	K6002	K6003	K6011	K6012	KD6015	KJ6008
Test Frequency (MHz)	60	60	60	60	60	60	60	450
Max. Noise Fig.[2] @ I_C (dB)	1.0	1.3	1.5	2.0	1.5	2.0	4.0	2.0
G_U (Max.) Typ. (dB)[3]	28	28	28	30	30	30	35	18
I_C (mA)	5.0	5.0	5.0	5.0	15.0	20.0	40.0	5.0
MODEL NO.	MA-42009	MA-42010	MA-42011	MA-42010	MA-42011	MA-42015	MA-42016	MA-42012
CASE STYLE[1]	509	509	509	510	510	510	510	510
KMC Model No.[4]	K6009	K6021	K6022	KD6021	——	KD6061	KD6062	KD6063
Test Frequency (MHz)	450	450	450	450	450	450	450	450
Max. Noise Fig.[2] @ I_C (dB)	2.5	3.0	3.5	3.5	4.0	4.0	4.5	5.0
G_U (Max.) Typ. (dB)[3]	14	15	15	20	20	20	20	20
I_C (mA)	5.0	20.0	20.0	40.0	40.0	60.0	60.0	60.0

NOTES:

1. Suffix indicates case style
2. V_{CE} = 10 volts.
3. $G_U(\text{Max})(\text{dB}) = 10 \log \frac{|S_{21E}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$
4. The KD package is no longer available and has been replaced by the ODS 510.

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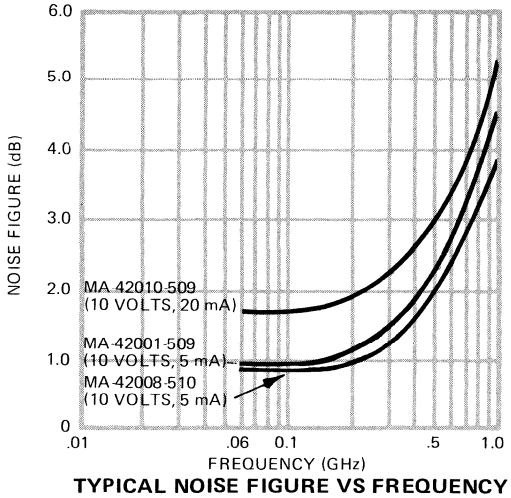
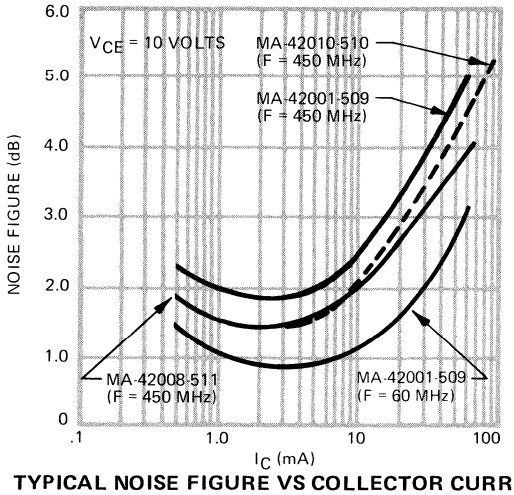
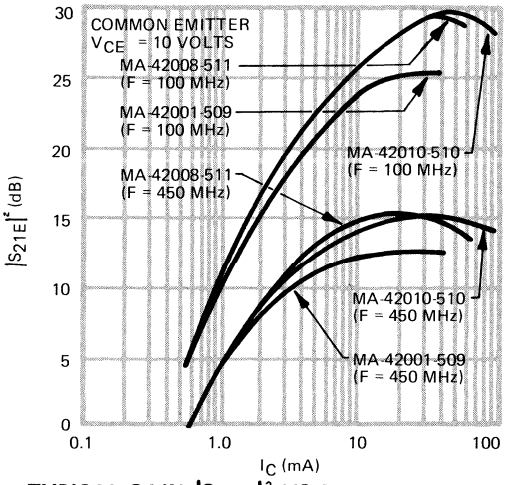


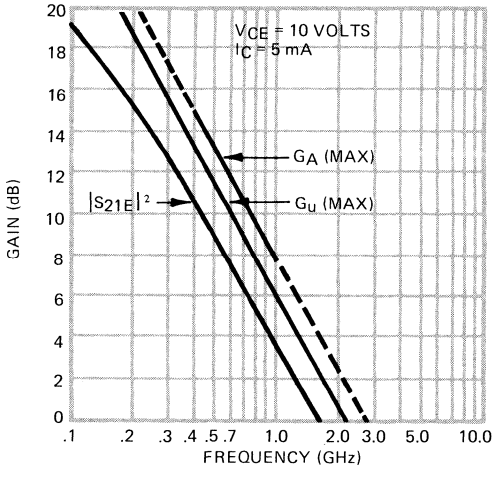
TYPICAL NOISE FIGURE VS FREQUENCY



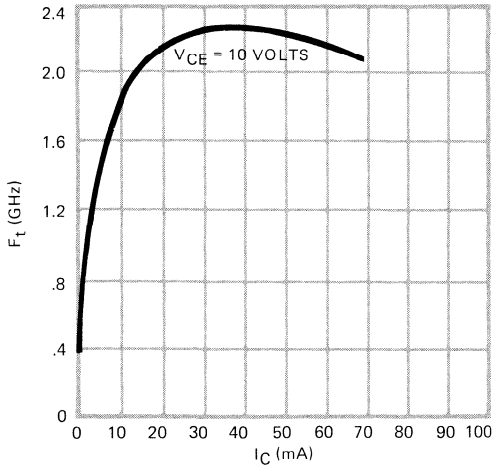
TYPICAL NOISE FIGURE VS COLLECTOR CURRENT



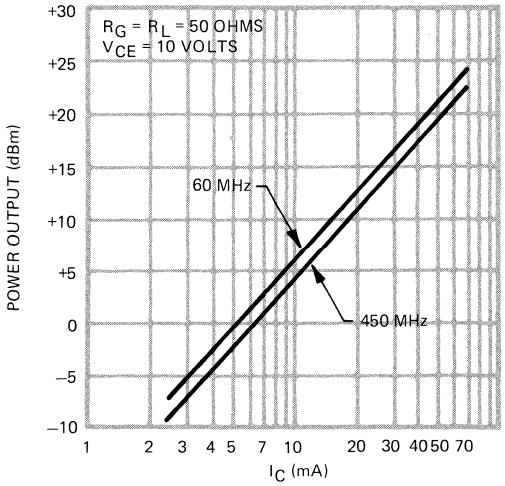
TYPICAL GAIN $|S_{21E}|^2$ VS COLLECTOR CURRENT



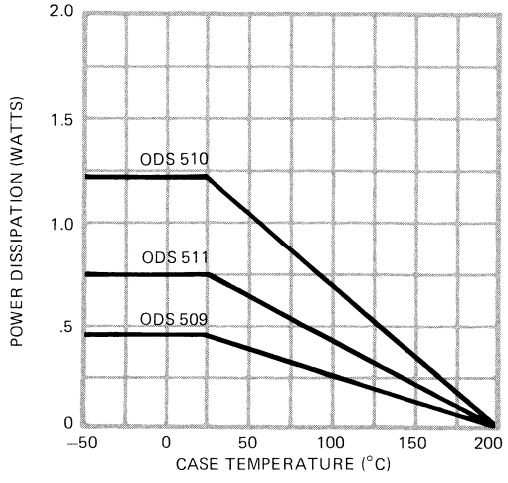
MA-42001-509 GAIN PARAMETERS VS FREQUENCY



TYPICAL F_T VS COLLECTOR CURRENT



TYPICAL POWER OUTPUT @ 1 dB COMPRESSION POINT VS COLLECTOR CURRENT



POWER DISSIPATION VS CASE TEMPERATURE

MA-42000 SERIES

specification sheet

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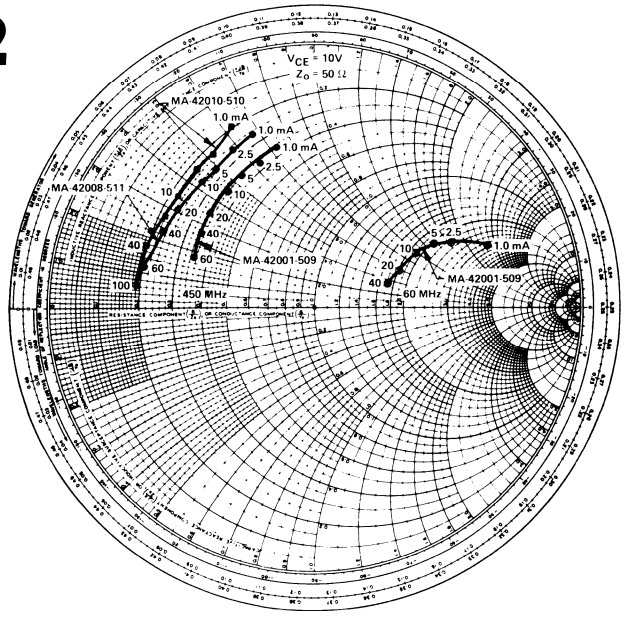
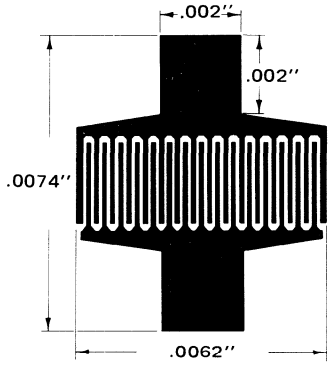


TYPICAL OPTIMUM GENERATOR IMPEDANCE VS CURRENT



GEOMETRY 60

ELECTRICAL CHARACTERISTICS (Case Temperature 25°C)

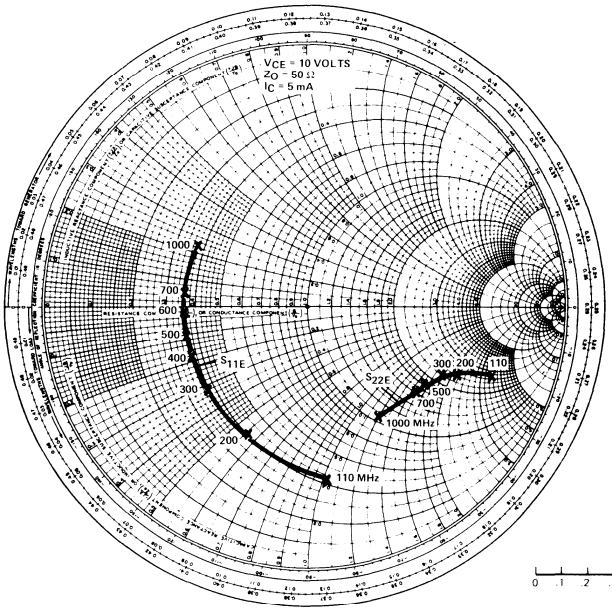
Symbol	Definition	Conditions	Min.	Typ.	Max.
BV_{CBO}	Collector base Breakdown voltage	I_C = 10 μA	20 V	25 V	
BV_{EBO}	Emitter base breakdown voltage	I_E = 10 μA	2.5 V	3.0 V	
I_{CBO}	Collector cut off current	V_{CB} = 10V			10 nA
h_{FE}	Current transfer ratio	V_{CE} = 10V, I_C = 5 mA	20		300
C_{CB}	Output Capacitance	V_{CB} = 15V			1.7 pF (509) 1.3 pF (510) 1.2 pF (511)

MAXIMUM RATING
(Case Temperature 25° C unless otherwise noted)

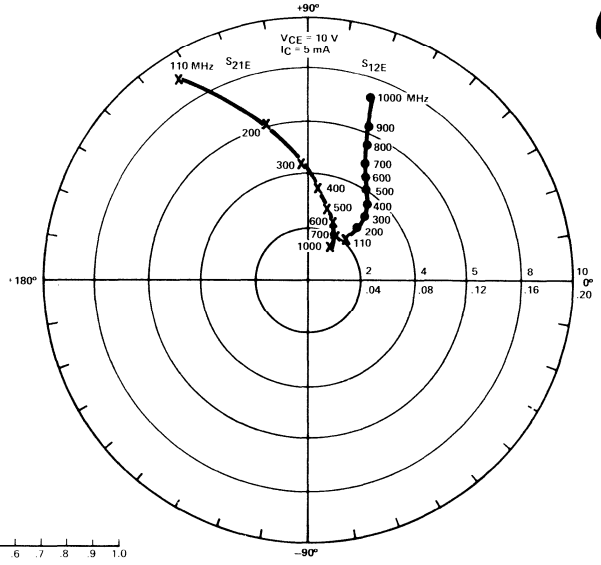
Total Device Power Dissipation	509 Case – 450 mW 510 Case – 1.2 W 511 Case – 750 mW
V_{CBO} Collector to Base Voltage	20 V
V_{EBO} Emitter to Base Voltage	3 V
Collector Current	125 mA
Storage Temperature	–65 to +200°C
Operation Junction Temperature	+200°C
Hermeticity	5 x $(10)^{-8}$ cc/sec of He
Lead Temperature (Soldering – 10 Seconds each lead)	250°C

ENVIRONMENTAL RATINGS PER MIL-STD-750

	Method	Level
Storage Temperature	1031	–65 to +200°C
Temperature Cycle	1051	10 cycles –65 to +200°C
Shock	2016	500 g's
Vibration	2056	15 g's
Constant Acceleration	2006	20,000 g's
Humidity	1021	10 days



TYPICAL S_{11E} AND S_{22E} VS FREQUENCY

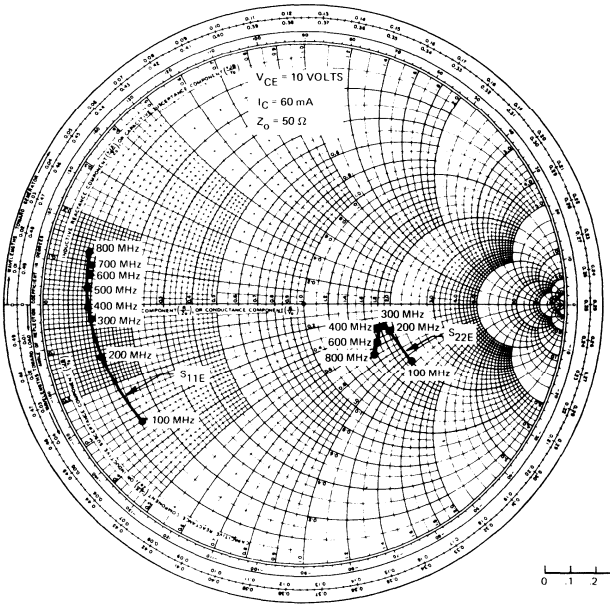


TYPICAL S_{12E} AND S_{21E} VS FREQUENCY

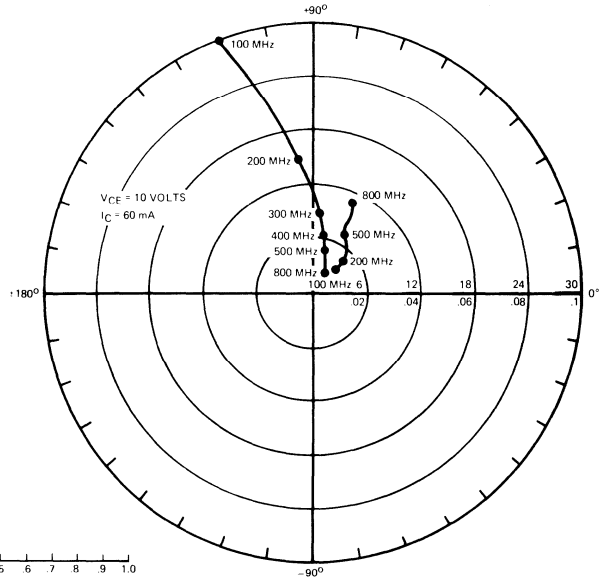
MA-42001-509
TYPICAL COMMON-EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 10 VOLTS, $Z_G = Z_L = 50\ \Omega$

FREQUENCY (MHz)	COLLECTOR CURRENT (mA)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
		$\lvert S_{11E}\rvert$	ϕS_{11E}	$\lvert S_{21E}\rvert$	ϕS_{21E}	$\lvert S_{12E}\rvert$	ϕS_{12E}	$\lvert S_{22E}\rvert$	ϕS_{22E}
110.0	5	.667	−83.6°	8.740	122.6°	.040	48.9°	.765	−21.7°
	20	.429	−116.4°	13.093	105.9°	.028	55.1°	.560	−23.7°
200.0	5	.551	−116.0°	6.026	104.7°	.054	45.7°	.649	−25.8°
	20	.381	−142.6°	8.057	92.8°	.041	60.3°	.481	−24.5°
300.0	5	.496	−138.8°	4.324	92.4°	.064	48.1°	.597	−28.4°
	20	.365	−158.9°	5.605	84.4°	.062	64.4°	.460	−26.4°
400.0	5	.475	−155.0°	3.455	83.1°	.070	50.9°	.578	−30.7°
	20	.364	−170.4°	4.387	76.9°	.074	65.6°	.456	−27.9°
500.0	5	.466	−167.2°	2.798	75.0°	.080	55.8°	.570	−32.4°
	20	.367	−178.8°	3.521	70.4°	.091	67.0°	.455	−29.2°
600.0	5	.467	−178.2°	2.388	69.1°	.088	59.9°	.551	−35.6°
	20	.373	173.9°	2.992	65.1°	.106	67.3°	.446	−30.6°
700.0	5	.470	174.0°	2.131	62.1°	.098	63.3°	.528	−38.6°
	20	.384	167.7°	2.652	59.0°	.121	67.4°	.427	−32.7°
800.0	5	.474	167.0°	1.878	57.3°	.114	65.4°	.511	−44.3°
	20	.392	163.7°	2.337	54.1°	.138	67.0°	.409	−37.4°
900.0	5	.469	161.1°	1.726	52.4°	.127	67.1°	.506	−50.4°
	20	.394	158.6°	2.131	50.0°	.152	66.2°	.406	−44.4°
1000.0	5	.464	153.6°	1.582	46.3°	.145	70.0°	.503	−56.4°
	20	.391	152.4°	1.953	44.1°	.169	67.0°	.410	−50.6°

specification sheet



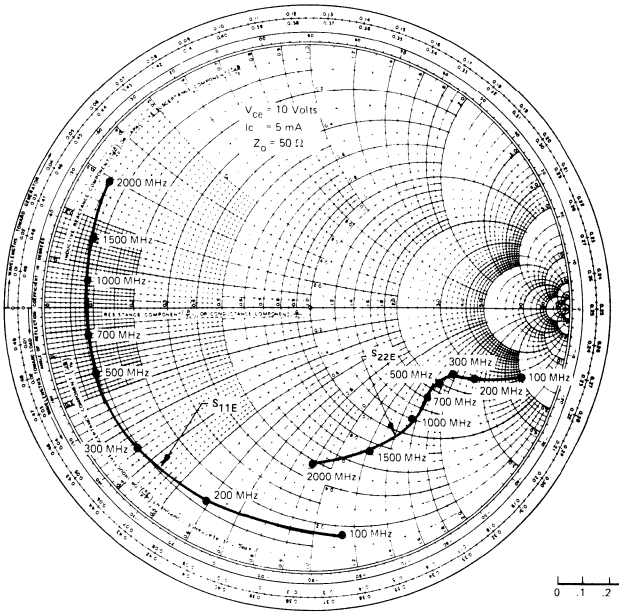
TYPICAL S_{11E} AND S_{22E} VS FREQUENCY



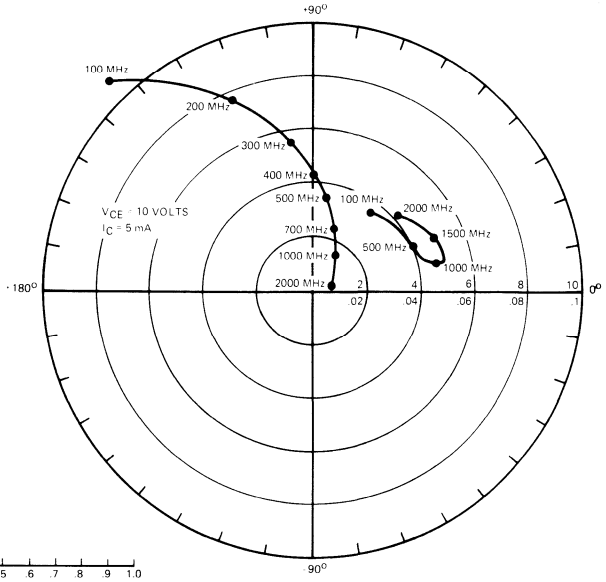
TYPICAL S_{12E} AND S_{21E} VS FREQUENCY

MA-42010-510
TYPICAL COMMON EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 10 VOLTS, $Z_G = Z_L$ = 50 Ω

FREQUENCY (MHz)	COLLECTOR CURRENT (mA)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
		S_{11E}	ϕS_{11E}	S_{21E}	ϕS_{21E}	S_{12E}	ϕS_{12E}	S_{22E}	ϕS_{22E}
100	20	0.78	−113°	26.25	123°	0.02	49°	0.63	−28°
	60	0.76	−143°	30.01	111°	0.01	45°	0.49	−30°
200	20	0.80	−148°	13.93	103°	0.02	36°	0.42	−29°
	60	0.80	−164°	14.54	96°	0.01	43°	0.34	−22°
300	20	0.81	−165°	8.64	91°	0.02	32°	0.37	−28°
	60	0.81	−174°	8.81	86°	0.02	46°	0.32	−20°
400	20	0.81	−171°	6.42	85°	0.03	36°	0.35	−28°
	60	0.82	−178°	6.38	80°	0.02	50°	0.31	−21°
500	20	0.82	−177°	4.95	79°	0.03	39°	0.34	−29°
	60	0.84	178°	4.92	75°	0.02	56°	0.31	−23°
600	20	0.81	179°	4.10	73°	0.03	43°	0.34	−32°
	60	0.82	174°	4.11	68°	0.03	59°	0.32	−26°
700	20	0.80	175°	3.37	67°	0.03	46°	0.34	−35°
	60	0.82	172°	3.38	63°	0.03	63°	0.32	−29°
800	20	0.83	171°	2.91	62°	0.04	46°	0.33	−39°
	60	0.85	168°	2.82	58°	0.03	61°	0.33	−33°
900	20	0.90	175°	2.38	62°	0.04	51°	0.35	−42°
	60	0.92	172°	2.32	59°	0.03	64°	0.34	−37°
1000	20	0.82	165°	2.37	54°	0.04	53°	0.36	−45°
	60	0.83	162°	2.28	49°	0.04	64°	0.35	−40°



TYPICAL S_{11E} AND S_{22E} VS FREQUENCY



TYPICAL S_{12E} AND S_{21E} VS FREQUENCY

MA-42008-511
TYPICAL COMMON EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 10 VOLTS, $Z_G = Z_L$ = 50 Ω

FREQUENCY (MHz)	COLLECTOR CURRENT (mA)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
		S_{11E}	ϕS_{11E}	S_{21E}	ϕS_{21E}	S_{12E}	ϕS_{12E}	S_{22E}	ϕS_{22E}
100	5	0.88	− 82°	10.74	135°	0.04	51°	0.84	−20°
	20	0.81	−131°	19.07	113°	0.02	37°	0.57	−27°
300	5	0.85	−141°	5.54	100°	0.05	22°	0.60	−26°
	20	0.86	−166°	7.61	89°	0.02	26°	0.42	−25°
500	5	0.85	−161°	3.45	85°	0.05	12°	0.56	−32°
	20	0.83	−176°	4.57	77°	0.03	30°	0.40	−30°
700	5	0.83	−173°	2.46	72°	0.05	11°	0.55	−39°
	20	0.84	177°	3.23	66°	0.03	38°	0.41	−35°
900	5	0.85	179°	1.91	62°	0.05	11°	0.58	−45°
	20	0.82	171°	2.42	58°	0.03	40°	0.43	−42°
1100	5	0.87	173°	1.58	54°	0.05	14°	0.56	−52°
	20	0.86	166°	2.05	50°	0.03	47°	0.43	−49°
1300	5	0.87	168°	1.31	44°	0.04	17°	0.57	−61°
	20	0.88	162°	1.90	40°	0.04	52°	0.44	−56°
1500	5	0.86	163°	1.13	35°	0.04	21°	0.59	−69°
	20	0.86	158°	1.42	31°	0.04	55°	0.47	−65°
1700	5	0.86	158°	1.01	28°	0.04	29°	0.59	−76°
	20	0.86	154°	1.28	24°	0.05	59°	0.48	−72°
2000	5	0.88	150°	0.82	20°	0.04	40°	0.61	−89°
	20	0.89	146°	1.02	15°	0.05	61°	0.51	−85°

notes

specification sheet

npn silicon planar transistors

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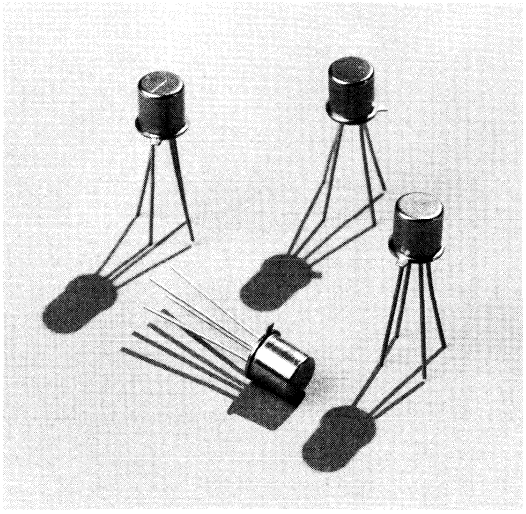
FEATURES

- LOW NOISE FIGURE AT LOW I_C (1.5 dB @ 1.0 mA)
- HIGH GAIN (23 dB TYPICAL @ 60 MHz)
- USEFUL TO 700 MHz
- LOW COST
- GOLD METALLIZATION
- HIGH RELIABILITY

DESCRIPTION

This series of NPN Silicon Planar Transistors is designed especially for low cost applications demanding low noise, high gain performance at VHF and UHF. Gold metallization employed in the construction of the device results in a rugged, highly reliable transistor.



APPLICATIONS

IF, VHF, UHF, TV and RF Amplifiers.

MA-42020 SERIES HIGH FREQUENCY SPECIFICATIONS

MODEL NO.	MA-42020	MA-42021	MA-42022	MA-42023	MA-42024	MA-42025	MA-42026	MA-42027	MA-42028
CASE STYLE	509	509	509	509	509	509	509	509	509
KMC Model No.	K2116 K2069	K2117 K2020	K2071 K2118	K2070	K2072	K2112	K2113	K2113	K2073
Test Frequency (MHz)	60	60	60	60	60	450	450	450	450
Noise Figure (dB)(max)	1.6	2.0	2.5	2.0	3.0	2.5	3.0	3.5	4.0
I_C (mA)[1]	1.5	1.5	1.5	1.5	1.5	1.0	1.0	1.0	1.5
G_u (max)[2] (Typ)(dB)	23	23	23	23	23	13	10	13	10

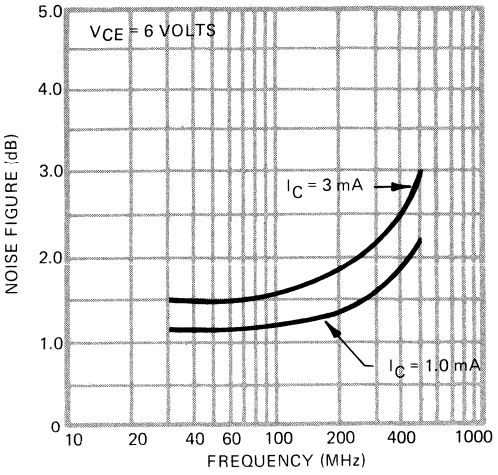
MODEL NO.	2N-5031	2N-3570	2N-3953	2N-5032	2N-3880	2N-3839	2N-3571	2N-5054	2N-3683	2N-5179	2N-5053	2N-3572
Test Frequency (MHz)	450	450	450	450	450	450	450	450	450	450	450	450
Noise Figure (dB)(max)	2.5	2.5	3.0	3.0	3.5	3.9	4.0	4.0	4.5	4.5	5.0	6.0
I_C (mA)[1]	1.0	1.5	1.0	1.0	1.5	1.5	2.0	2.0	1.5	2.0	2.0	2.0
G_u (max)[2] (dB)	10	10	10	10	10	10	10	10	10	10	10	10

NOTES:

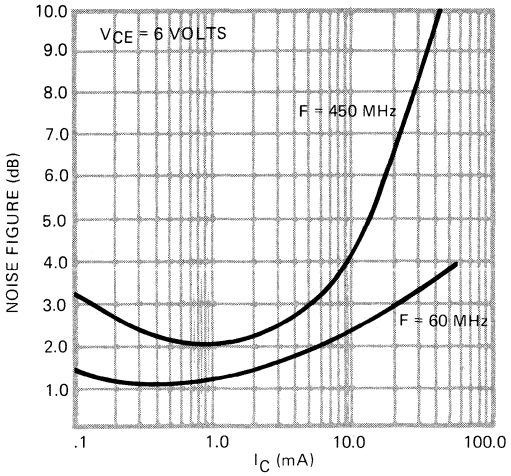
1. Test current for Noise Figure measurement, V_{CE} = 6 Volts.
2. G_u (Max.) may be derived from S-Parameter data; G_u (Max.)(dB)

$$= 10 \log \frac{|S_{21E}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$$

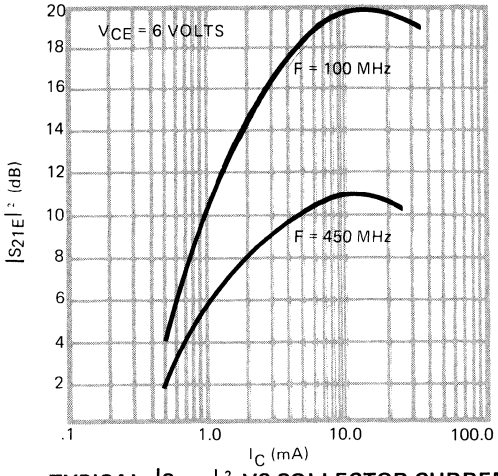
specification sheet



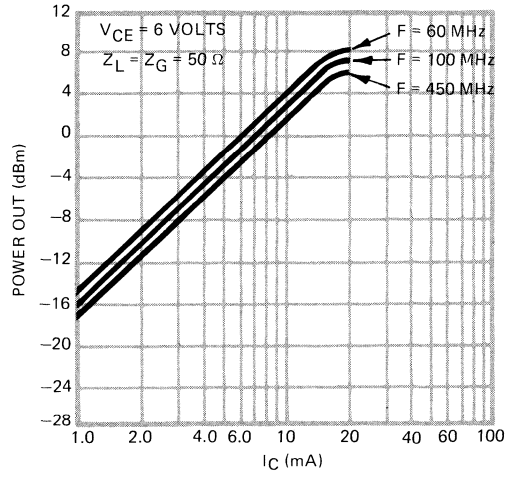
TYPICAL NOISE FIGURE VS FREQUENCY



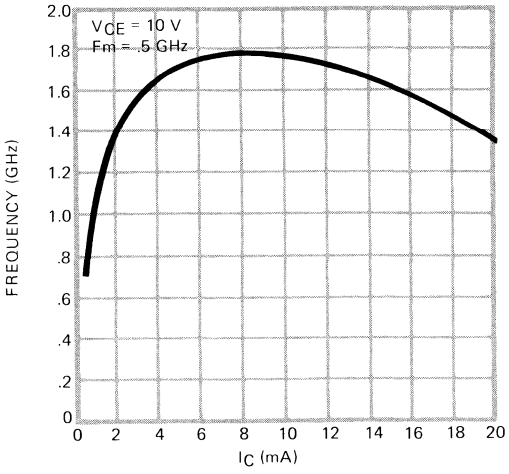
TYPICAL NOISE FIGURE VS COLLECTOR CURRENT



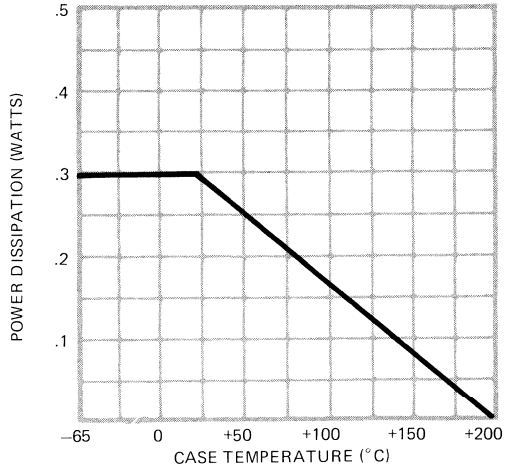
TYPICAL $|S_{21E}|^2$ VS COLLECTOR CURRENT



TYPICAL POWER OUTPUT @ 1 dB COMPRESSION VS COLLECTOR CURRENT

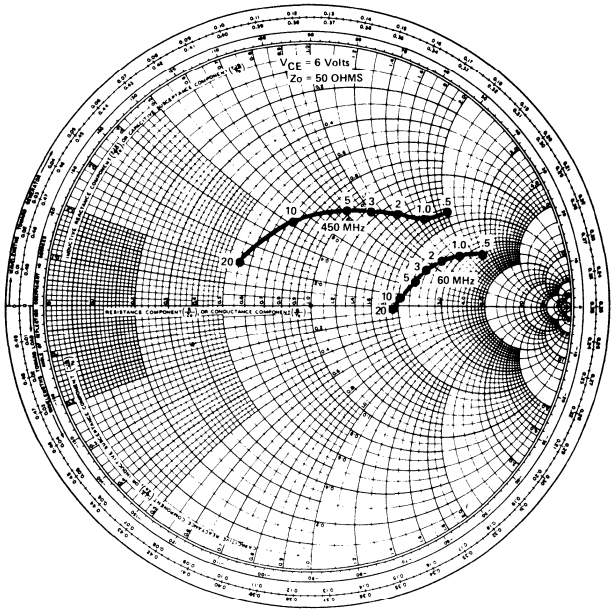


TYPICAL F_T VS COLLECTOR CURRENT

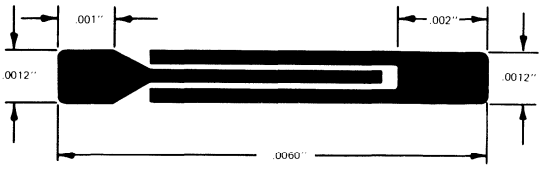


POWER DISSIPATION VS CASE TEMPERATURE

specification sheet



TYPICAL OPTIMUM SOURCE IMPEDANCE
VS COLLECTOR CURRENT



GEOMETRY 20

ELECTRICAL CHARACTERISTICS (25°C Ambient Temperature unless otherwise noted)

Symbol	Definition	Condition	Value
BV_{cbo}	Collector-base breakdown	Ic = 1 μA	30 V min.
BV_{ebo}	Emitter-base breakdown	Ie = 10 μA	2.5 V min.
I_{cbo}	Collector cut-off current	Vcb = 15 V	0.01 μA max.
h_{FE}	Current transfer ratio	Vce = 1 V	30 min.
		Ic = 3 mA	300 max.

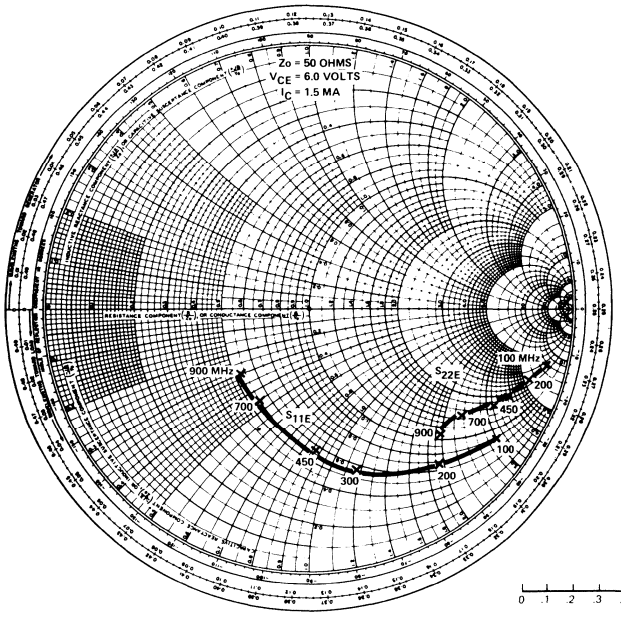
MAXIMUM RATINGS
(Case Temperature 25°C unless otherwise noted)

Total Device Power Dissipation	509 Case, 300 mW
Collector Current	50 mA
Storage Temperature	–65 to +200°C
Hermeticity	5 x $(10)^{-8}$ cc/sec of He
Operating Junction Temperature	+200°C
Lead Temperature (soldering – 10 seconds each lead)	265°C

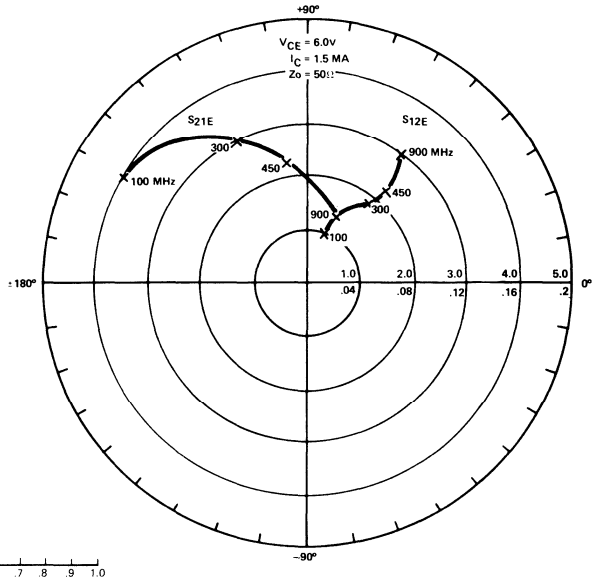
ENVIRONMENTAL RATINGS PER MIL-STD-750

	Method	Level
Storage Temperature	1031	–65 to +200°C
Temperature Cycle	1051	10 cycles –65 to +200°C
Shock	2016	500 g's
Vibration	2056	15 g's
Constant Acceleration	2006	20,000 g's
Humidity	1021	10 days

specification sheet



TYPICAL S_{11E} AND S_{22E} VS FREQUENCY



TYPICAL S_{12E} AND S_{21E} VS FREQUENCY

MA-42020 SERIES
TYPICAL COMMON-EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 6.0 VOLTS, $Z_G = Z_L = 50\ \Omega$

FREQUENCY (MHz)	COLLECTOR CURRENT (mA)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
		$\lvert S_{11E}\rvert$	ϕS_{11E}	$\lvert S_{21E}\rvert$	ϕS_{21E}	$\lvert S_{12E}\rvert$	ϕS_{12E}	$\lvert S_{22E}\rvert$	ϕS_{22E}
100	1.0	.91	−26°	3.2	152°	.04	73°	.96	−11°
	1.5	.88	−39°	3.9	149°	.04	71°	.95	−12°
	3.0	.75	−48°	6.5	136°	.04	70°	.89	−15°
	5.0	.67	−53°	8.2	128°	.03	69°	.84	−16°
200	1.0	.82	−43°	3.0	138°	.06	65°	.92	−16°
	1.5	.77	−48°	3.6	135°	.06	65°	.92	−16°
	3.0	.61	−65°	5.4	122°	.05	61°	.82	−18°
	5.0	.49	−77°	6.4	114°	.04	60°	.78	−18°
300	1.0	.69	−64°	2.5	120°	.08	54°	.89	−21°
	1.5	.63	−70°	3.0	117°	.07	52°	.84	−23°
	3.0	.45	−89°	4.0	105°	.06	55°	.76	−22°
	5.0	.37	−100°	4.5	99°	.06	58°	.72	−21°
400	1.0	.62	−76°	2.3	110°	.09	51°	.84	−25°
	1.5	.56	−81°	2.6	108°	.09	50°	.81	−26°
	3.0	.39	−100°	3.9	97°	.07	56°	.79	−24°
	5.0	.32	−111°	3.7	91°	.06	60°	.71	−23°
450	1.0	.56	−80°	2.1	107°	.09	49°	.84	−26°
	1.5	.55	−86°	2.2	102°	.08	51°	.80	−26°
	3.0	.39	−104°	2.8	92°	.07	55°	.74	−25°
	5.0	.32	−117°	3.4	87°	.06	60°	.72	−23°
500	1.0	.54	−87°	2.0	101°	.10	49°	.82	−28°
	1.5	.49	−93°	2.2	97°	.09	50°	.78	−28°
	3.0	.34	−112°	2.8	87°	.08	56°	.73	−26°
	5.0	.29	−123°	3.0	83°	.07	61°	.70	−24°
600	1.0	.46	−102°	1.7	91°	.11	47°	.77	−31°
	1.5	.41	−108°	1.9	88°	.10	49°	.74	−31°
	3.0	.30	−126°	2.3	79°	.09	57°	.70	−28°
	5.0	.26	−138°	2.5	76°	.09	63°	.68	−26°
700	1.0	.44	−111°	1.6	85°	.11	47°	.72	−34°
	1.5	.38	−117°	1.8	83°	.11	50°	.72	−33°
	3.0	.29	−135°	2.1	75°	.10	60°	.68	−30°
	5.0	.25	−145°	2.2	70°	.09	64°	.67	−28°

NOTE: Full S-Parameter measurements on an individual unit basis are available at a nominal charge.

specification sheet

npn silicon planar transistors

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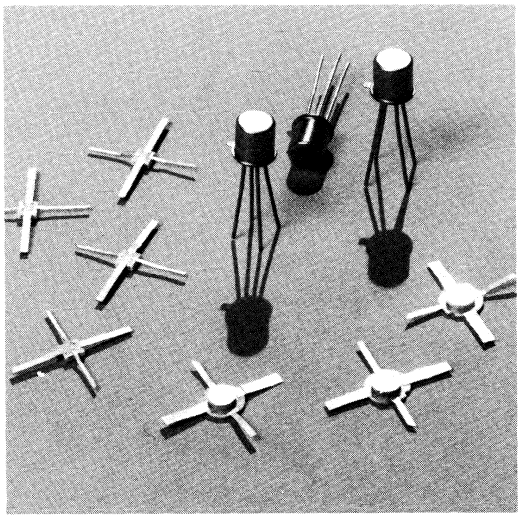
FEATURES

- HIGH GAIN (18 dB @ 450 MHz)
- GOLD METALLIZATION
- LOW NOISE (2.0 dB @ 450 MHz)
- LOW COST

DESCRIPTION

The MA-42050 series of npn silicon planar transistors is designed to give high gain and low noise figure characteristics in amplifier applications. The refractory gold metallization techniques employed in the construction of the device results in a rugged, highly reliable transistor.

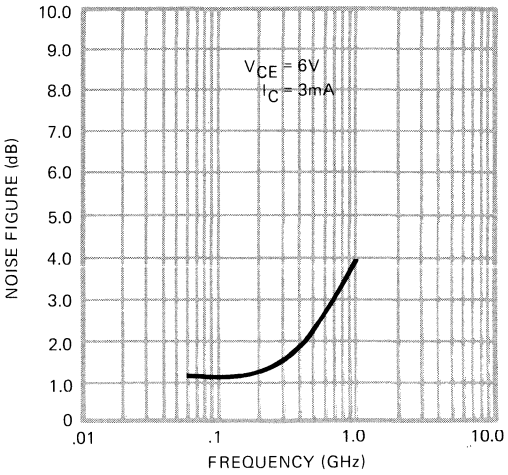


APPLICATIONS

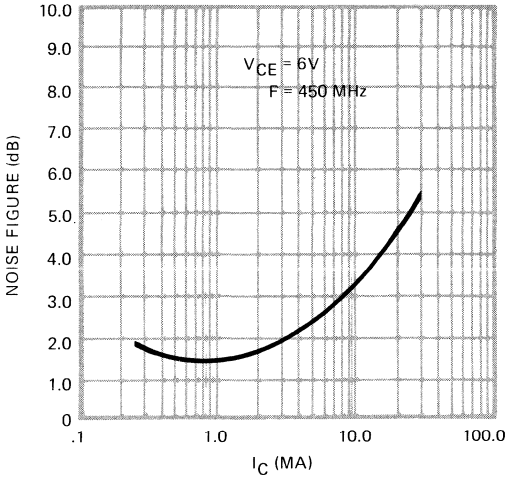
IF, VHF, UHF, TV and RF amplifiers and oscillators.

MA-42050 SERIES R.F.SPECIFICATIONS

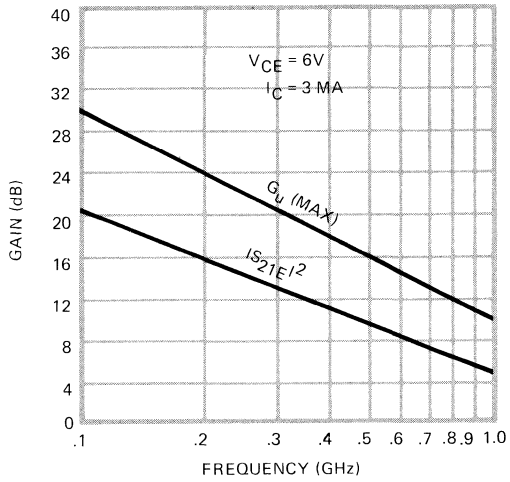
MODEL NO.	MA-42051	MA-42052	MA-42056
CASE STYLE	509, 510, 511	509, 510, 511	510, 511
KMC Model No.	K5511	K5512	K5526
Test Frequency (MHz)	450	450	1000
Noise Figure (max) @ I_C (dB)	2.2	2.5	4.5
I_C (mA)	3.0	3.0	3.0
G_u (max) (Typ.) (dB)	18	18	11
1 dB Compression Point (dBm)	+1	+1	0



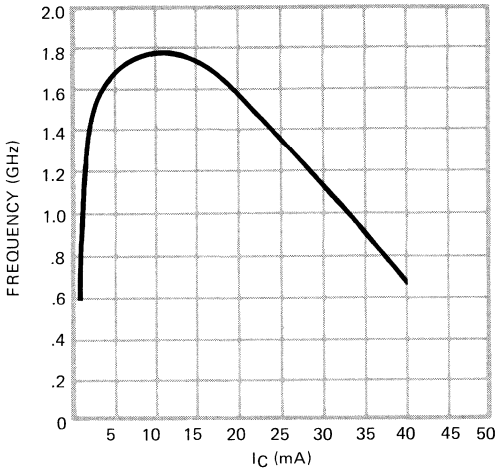
TYPICAL OPTIMUM NOISE FIGURE VS FREQUENCY



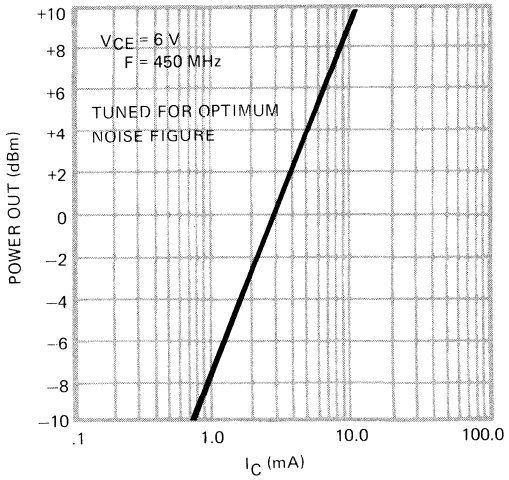
TYPICAL OPTIMUM NOISE FIGURE VS VS COLLECTOR CURRENT



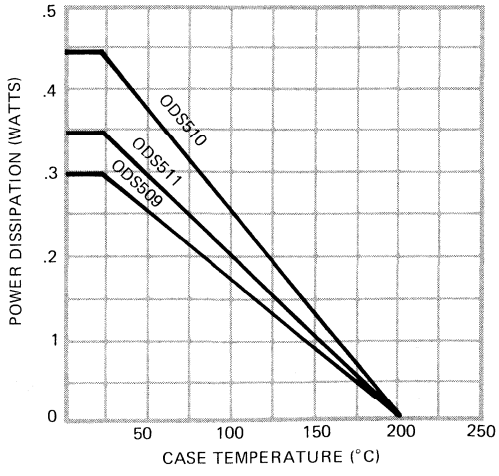
TYPICAL GAIN PARAMETERS VS FREQUENCY



TYPICAL F_T VS COLLECTOR CURRENT

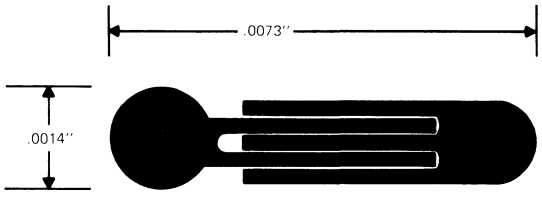


TYPICAL POWER OUT AT 1 dB COMPRESSION POINT VS COLLECTOR CURRENT



POWER DISSIPATION VS CASE TEMPERATURE

specification sheet



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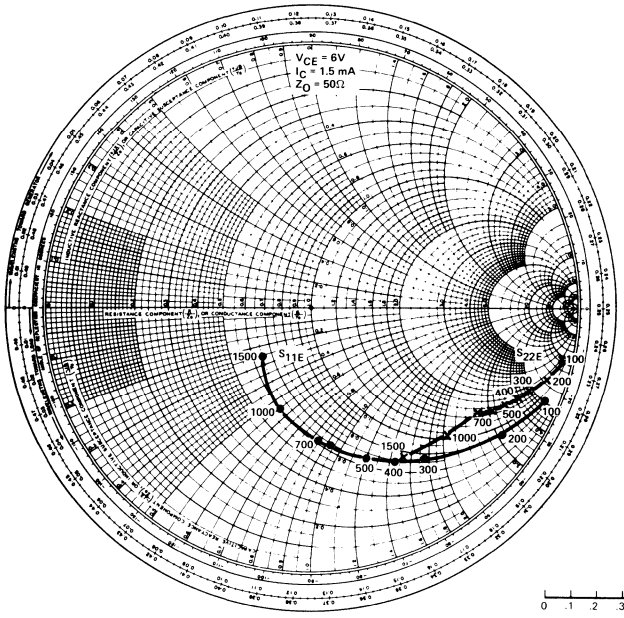
ELECTRICAL CHARACTERISTICS (Case Temperature 25°C)

Symbol	Definition	Conditions	Min.	Max.
BV_{CBO}	Collector base breakdown	I_C = 10 μA	20 V	
BV_{EBO}	Emitter-base breakdown	I_E = 10 μA	2.5 V	
I_{CBO}	Collector cut-off current	V_{CB} = 10 V		0.05 μA
h_{FE}	Current transfer ratio	V_{CE} = 1 V I_C = 3 mA	20	
C_{OB}	Output capacitance	V_{CE} = 10 V		0.75 pF

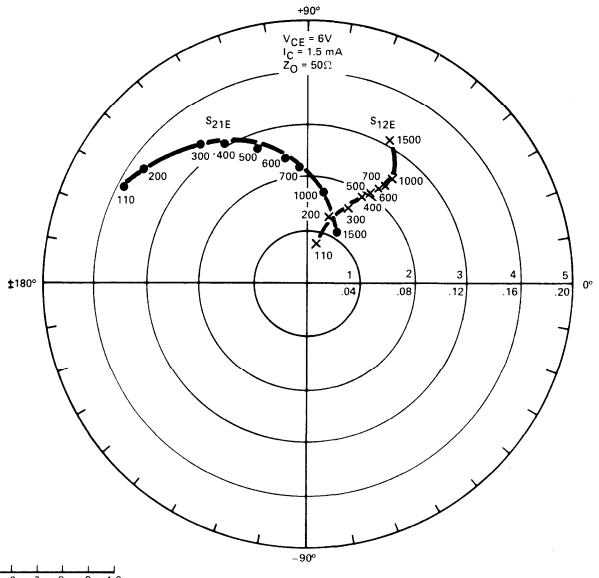
MAXIMUM RATING
(Case Temperature 25°C unless otherwise noted)

Total Device Power	509 Case – 300 mW 510 Case – 450 mW 511 Case – 350 mW
V_{CBO} Collector to Base Voltage	20 V
V_{EBO} Emitter to Base Voltage	2.5 V
Collector Current	40 mA
Storage Temperature	–65 to +200°C
Hermeticity	5 x $(10)^{-8}$ cc/sec of He
Operating Junction Temperature	+200°C
Lead Temperature (Soldering – 10 Seconds each lead)	230°C

specification sheet



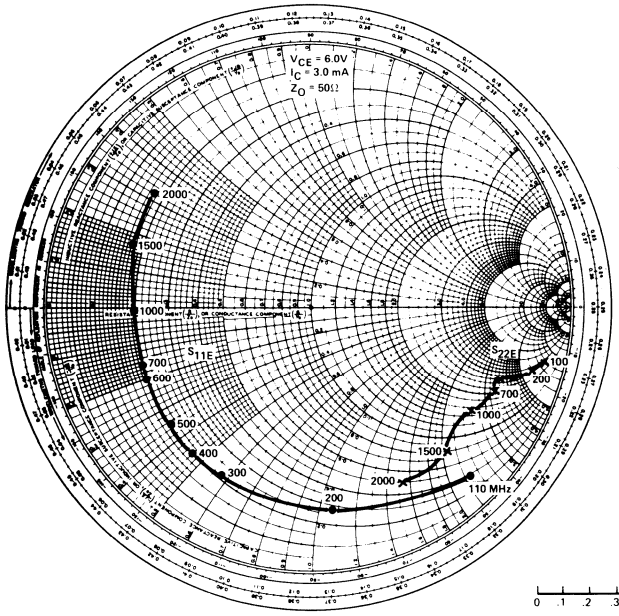
TYPICAL S_{11E} AND S_{22E} VS FREQUENCY



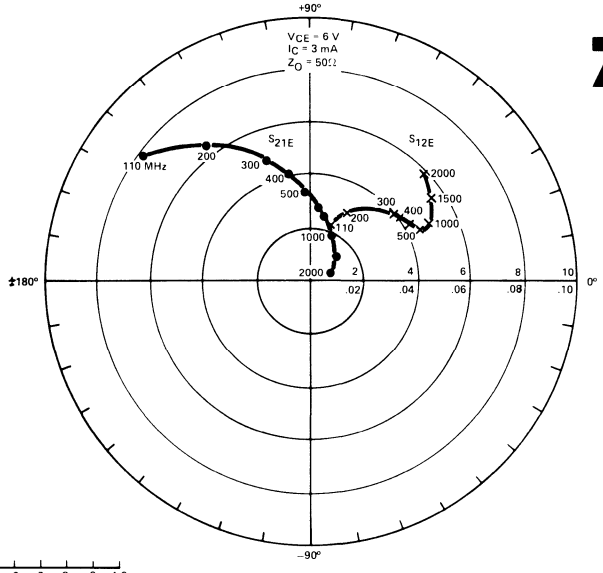
TYPICAL S_{21E} AND S_{12E} VS FREQUENCY

MA-42051-509
TYPICAL COMMON EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
I_C = 1.5 mA, V_{CE} = 6.0 VOLTS, $Z_G = Z_L$ = 50 Ω

FREQUENCY (MHz)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
	$\|S_{11E}\|$	ϕS_{11E}	$\|S_{21E}\|$	ϕS_{21E}	$\|S_{12E}\|$	ϕS_{12E}	$\|S_{22E}\|$	ϕS_{22E}
110.0	.944	−22.4°	3.824	152.6°	.035	74.0°	.962	−10.9°
200.0	.860	−33.8°	3.744	144.3°	.045	68.9°	.938	−14.1°
300.0	.720	−52.8°	3.289	126.8°	.065	61.7°	.878	−19.8°
400.0	.677	−60.0°	3.055	119.2°	.073	58.4°	.854	−22.8°
500.0	.621	−69.6°	2.671	109.9°	.081	56.2°	.818	−25.9°
600.0	.534	−81.0°	2.400	100.0°	.089	53.9°	.770	−28.8°
700.0	.493	−85.4°	2.288	94.4°	.092	53.3°	.752	−31.0°
800.0	.447	−96.2°	2.000	87.8°	.101	52.7°	.724	−35.6°
900.0	.425	−100.4°	1.866	83.3°	.105	53.2°	.711	−38.6°
1000.0	.398	−105.3°	1.743	77.9°	.108	54.5°	.716	−42.1°
1100.0	.361	−110.8°	1.591	74.0°	.115	55.9°	.711	−45.2°
1200.0	.339	−114.1°	1.504	70.3°	.116	56.4°	.705	−46.7°
1300.0	.299	−121.9°	1.365	63.5°	.121	58.6°	.691	−50.5°
1400.0	.280	−127.6°	1.285	61.3°	.123	58.1°	.671	−54.5°
1500.0	.259	−132.9°	1.268	58.5°	.124	61.1°	.661	−57.6°



TYPICAL S_{11E} AND S_{22E} VS FREQUENCY



TYPICAL S_{12E} AND S_{21E} VS FREQUENCY

MA-42051-510
TYPICAL COMMON EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
I_C = 3.0 mA, V_{CE} = 6.0 VOLTS, $Z_G = Z_L$ = 50 Ω

FREQUENCY (MHz)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
	$\|S_{11E}\|$	ϕS_{11E}	$\|S_{21E}\|$	ϕS_{21E}	$\|S_{12E}\|$	ϕS_{12E}	$\|S_{22E}\|$	ϕS_{22E}
110.0	.877	−46.9°	7.778	142.1°	.021	71.0°	.926	−12.8°
200.0	.771	−83.9°	6.312	126.3°	.031	50.2°	.880	−14.9°
300.0	.719	−117.9°	4.755	108.8°	.040	36.1°	.821	−19.4°
400.0	.710	−129.0°	4.141	101.2°	.041	34.9°	.810	−19.3°
500.0	.691	−141.3°	3.406	92.5°	.043	29.1°	.781	−20.7°
600.0	.678	−156.1°	2.807	81.1°	.045	27.9°	.775	−23.3°
700.0	.674	−161.3°	2.543	78.1°	.045	27.4°	.775	−24.2°
800.0	.695	−171.3°	2.178	68.5°	.046	27.5°	.737	−29.5°
900.0	.705	−174.5°	2.032	66.8°	.046	27.6°	.773	−28.3°
1000.0	.597	−179.9°	1.884	61.8°	.047	28.4°	.744	−31.8°
1100.0	.701	172.7°	1.664	56.3°	.048	27.7°	.742	−37.2°
1200.0	.708	172.0°	1.589	53.0°	.048	29.9°	.749	−37.2°
1300.0	.704	164.6°	1.401	46.1°	.060	29.4°	.758	−42.3°
1400.0	.694	163.8°	1.354	47.5°	.060	31.1°	.758	−42.9°
1500.0	.695	158.7°	1.255	39.5°	.063	35.4°	.785	−45.9°
1600.0	.706	151.6°	1.188	32.6°	.062	36.3°	.784	−50.7°
1700.0	.707	150.4°	1.114	30.8°	.066	38.3°	.773	−51.0°
1800.0	.712	145.1°	1.152	40.3°	.069	41.2°	.771	−55.5°
1900.0	.714	144.1°	.949	27.3°	.068	41.8°	.790	−57.9°
2000.0	.726	143.1°	.936	19.6°	.058	43.2°	.754	−61.7°

notes

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specification sheet

npn silicon planar transistors

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FEATURES

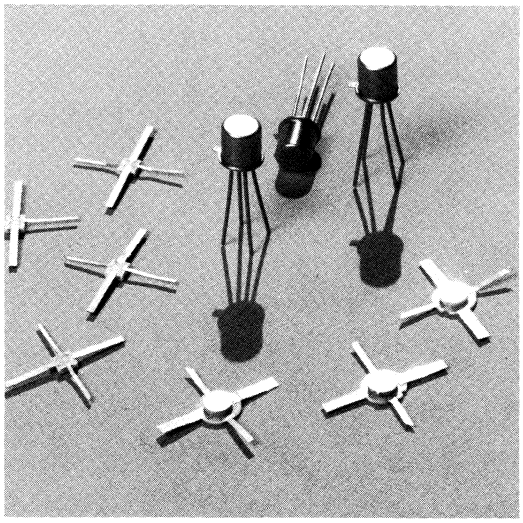
- LOW NOISE FIGURE (1.5 dB MAX @ 450 MHz)
- WIDE DYNAMIC RANGE (+25 dBm 1 dB COMPRESSION POINT)
- HIGH GAIN (14 dB @ 2 GHz)
- GOLD METALLIZATION
- LOW COST
- HIGH RELIABILITY
- ION IMPLANTED FOR OPTIMUM PERFORMANCE

DESCRIPTION

The MA-42110 series is designed to give very low noise figure and wide dynamic range up to approximately 4 GHz. Gold metallization employed in the construction of the device results in a rugged, highly reliable transistor.

APPLICATIONS

RF and IF amplifiers at frequencies up to 4 GHz.



MA-42110 SERIES RF SPECIFICATIONS (Case Temperature 25°C)

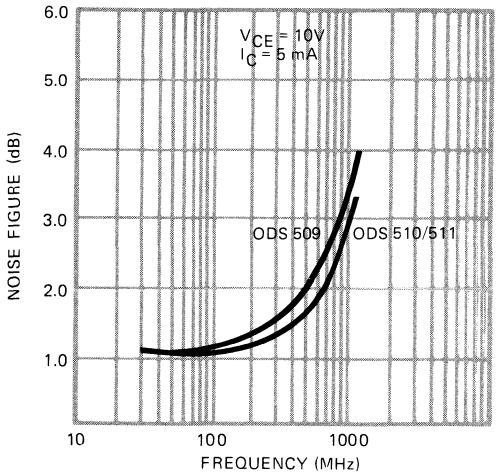
MODEL NO.	MA42111	MA42111	MA42111	MA42112	MA42112	MA42113	MA42113
CASE STYLE	509	510	511	509	510/511	509	510/511
Test Frequency (MHz)	450	450	450	450	450	450	450
Max. Noise[1] Fig. @ I_c (dB)	1.5	1.5	1.5	1.8	1.8	2.1	2.1
G_u (max)[2] Typ (dB)	14.0	17.0	19.0	14	17/19	14	17/19
1 dB Compression Point (dBm)	0	0	0	0	0	0	0
$\|S_{21E}\|^2$ min[2] (dB)	13.0	15.5	16.0	13.0	15.5/16	13.0	15.5/16
Typical Gain (Ga) @ Optimum N.F.[1] (dB)	13.0	15.0	15.0	13	15/15	13	15/15

ELECTRICAL CHARACTERISTICS (Case Temperature 25°C)

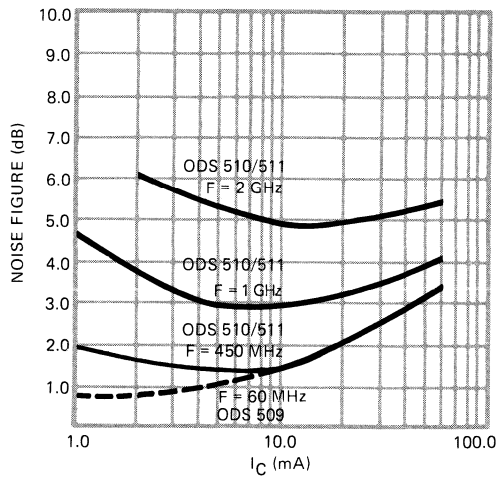
Symbol	Definition	Conditions	Min.	Typ.	Max.
BV_{CBO}	Collector base Breakdown voltage	$I_C = 10\mu A$	20 V	25 V	
BV_{EBO}	Emitter base breakdown voltage	$I_E = 10\mu A$	1.5 V	3.0 V	
I_{CBO}	Collector cut off current	$V_{CB} = 10$ V			10 nA
h_{FE}	Current transfer ratio	$V_{CE} = 10$ V, $I_C = 5$ mA	20		300
C_{CB}	Output Capacitance	$V_{CB} = 5$ V			1.7 pF (509) 1.3 pF (510) 1.2 pF (511)

NOTES

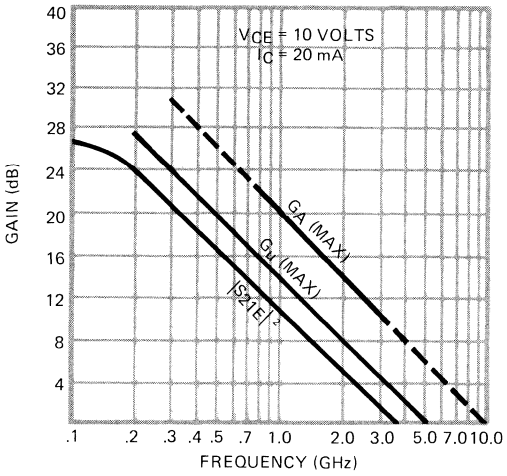
1. $V_{CE} = 10V$, $I_C = 5$ mA, frequency = 450 MHz.
2. $V_{CE} = 10V$, $I_C = 20$ mA, frequency = 450 MHz.
3. G_u (Max.) (dB) = 10 Log $\dfrac{|S_{21E}|^2}{(1-|S_{11}|^2)\ (1-|S_{22}|^2)}$



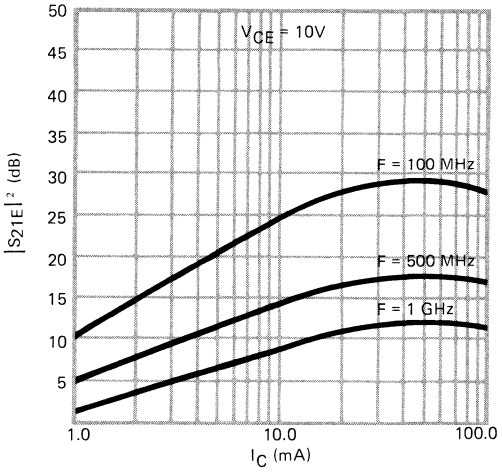
TYPICAL NOISE FIGURE VS FREQUENCY



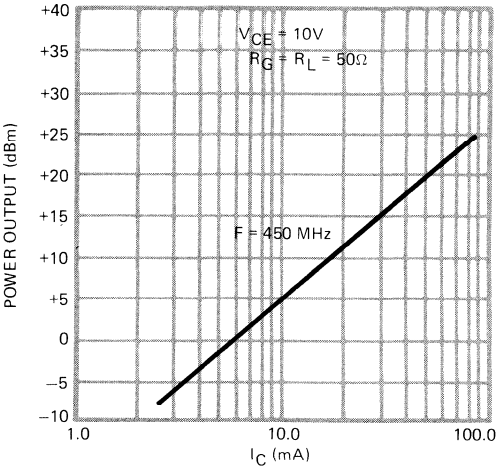
TYPICAL NOISE FIGURE VS COLLECTOR CURRENT



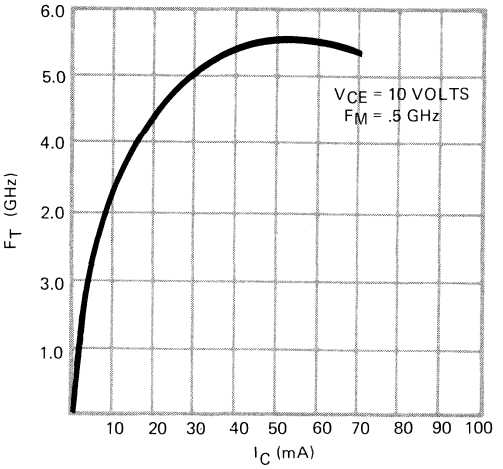
TYPICAL GAIN PARAMETERS VS FREQUENCY



TYPICAL $|S_{21E}|^2$ VS COLLECTOR CURRENT

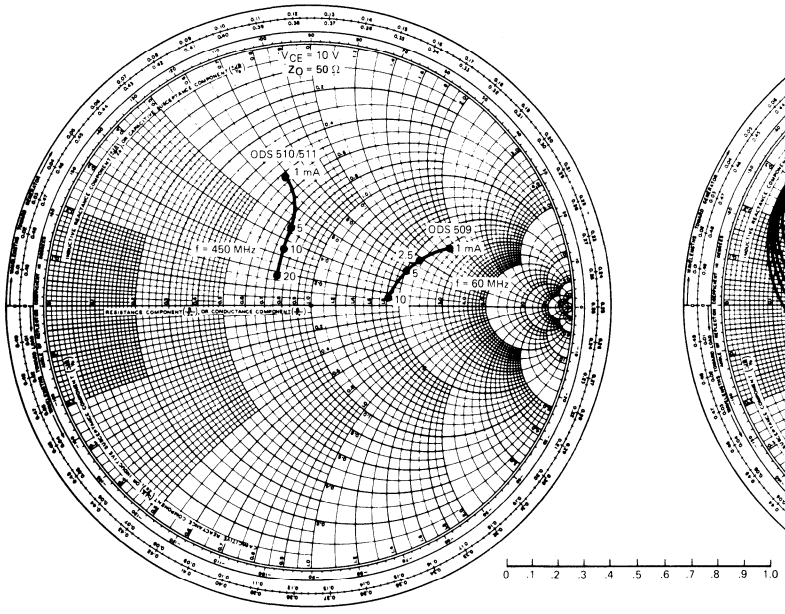


TYPICAL POWER OUTPUT AT 1 dB COMPRESSION POINT VS COLLECTOR CURRENT

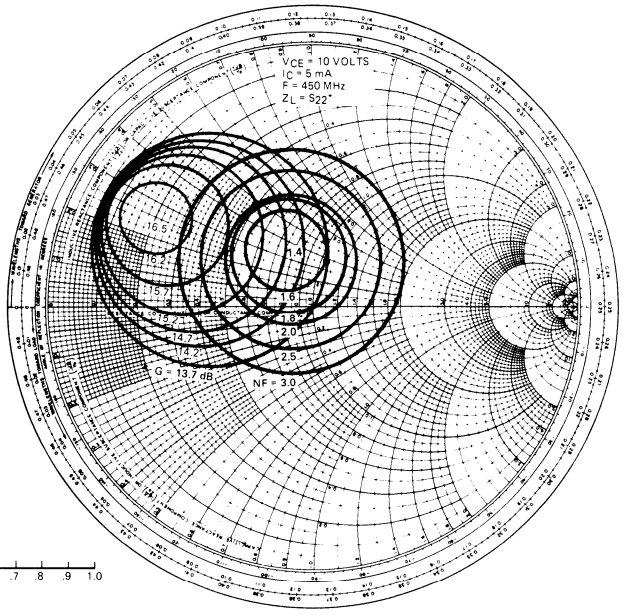


TYPICAL F_T VS COLLECTOR CURRENT

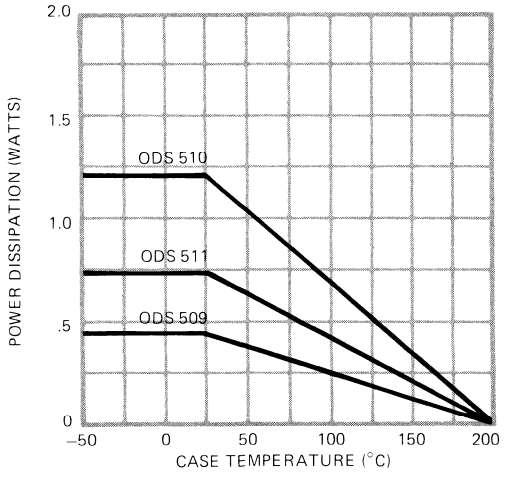
specification sheet



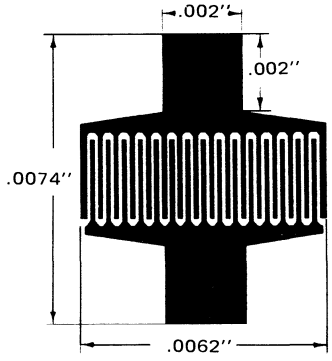
TYPICAL OPTIMUM GENERATOR IMPEDANCE VS COLLECTOR CURRENT



TYPICAL CONSTANT GAIN AND N.F. CIRCLES



POWER DISSIPATION VS CASE TEMPERATURE



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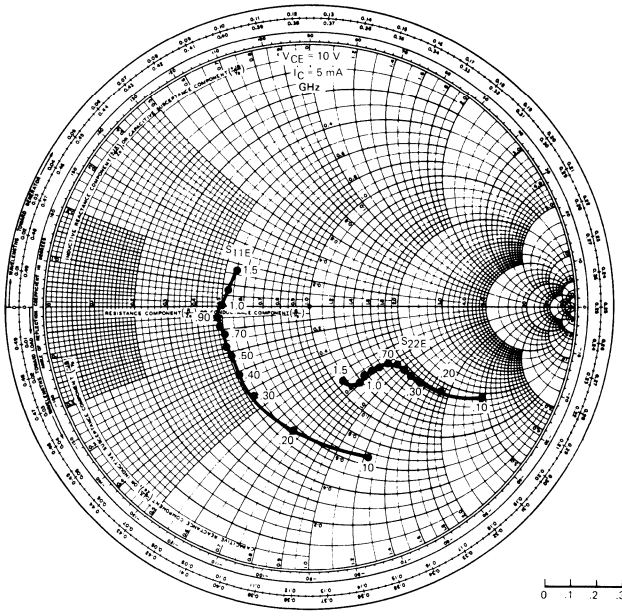
MAXIMUM RATING
(Case Temperature 25°C unless otherwise noted)

Total Device Power Dissipation	509 Case – 450 mW 510 Case – 1.2 W 511 Case – 750 mW
V_{CBO} Collector to Base Voltage	20 V
V_{EBO} Emitter to Base Voltage	2.5 V
Collector Current	125 mA
Storage Temperature	–65 to +200°C
Operating Junction Temperature	+200°C
Hermeticity	5 x $(10)^{-8}$ cc/sec of He
Lead Temperature (Soldering – 10 Seconds each lead)	250°C

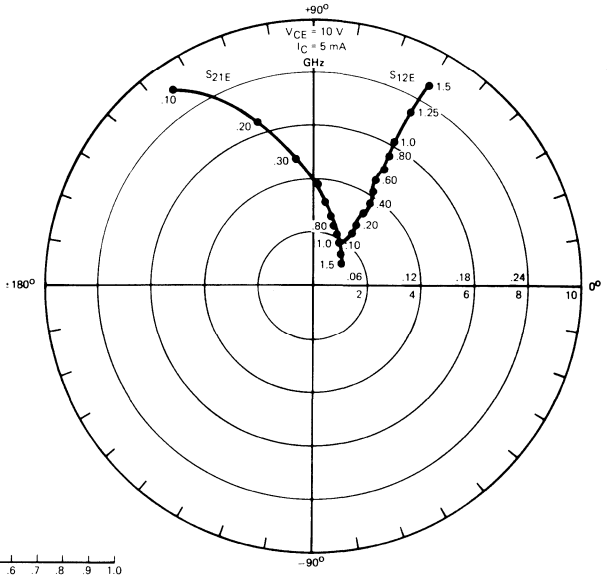
ENVIRONMENTAL RATINGS PER MIL-STD-750

	Method	Level
Storage Temperature	1031	–65 to +200°C
Temperature Cycle	1051	10 cycles –65 to +200°C
Shock	2016	500 g's
Vibration	2056	15 g's
Constant Acceleration	2006	20,000 g's
Humidity	1021	10 days

specification sheet



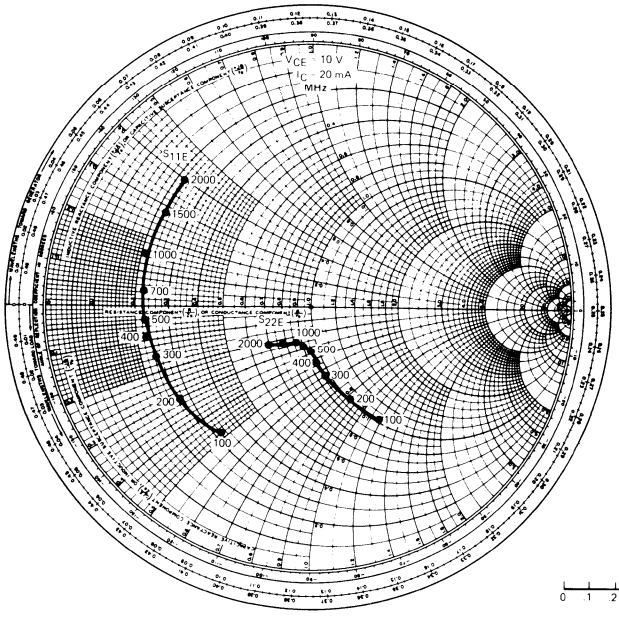
TYPICAL S_{11E} AND S_{22E} VS FREQUENCY



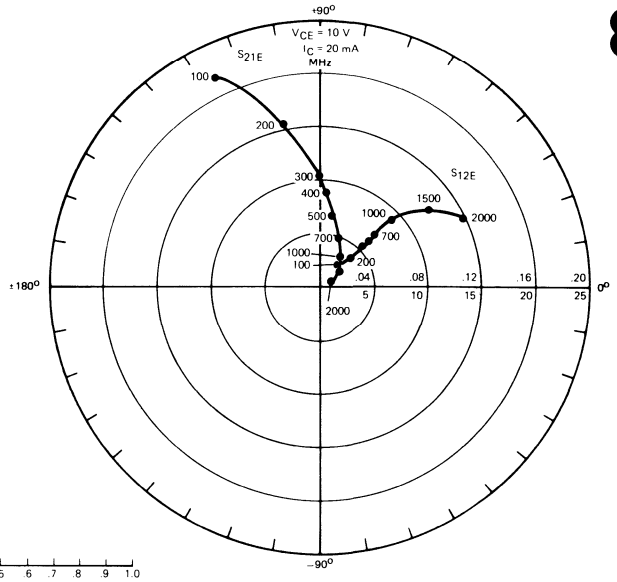
TYPICAL S_{12E} AMD S_{21E} VS FREQUENCY

MA-42111-509
TYPICAL COMMON EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 10 VOLTS, $Z_G = Z_L$ = 50 Ω

FREQUENCY (MHz)	COLLECTOR CURRENT (mA)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
		S_{11E}	ϕS_{11E}	S_{21E}	ϕS_{21E}	S_{12E}	ϕS_{12E}	S_{22E}	ϕS_{22E}
110.0	5	0.625	− 68.2°	9.154	126.1°	0.056	58.3°	0.725	−27.7°
	20	0.343	− 92.1°	14.427	110.1°	0.044	66.5°	0.473	−39.0°
	40	0.284	− 99.0°	15.208	105.9°	0.039	70.1°	0.408	−39.3°
250.0	5	0.436	−108.4°	5.537	102.5°	0.078	55.5°	0.536	−35.3°
	20	0.238	−128.0°	7.612	93.0°	0.073	68.5°	0.323	−40.2°
	40	0.202	−133.8°	7.845	90.8°	0.073	70.8°	0.283	−39.0°
450.0	5	0.330	−142.5°	3.467	83.0°	0.109	57.4°	0.460	−37.5°
	20	0.192	−158.2°	4.564	79.3°	0.116	68.7°	0.284	−37.6°
	40	0.170	−163.9°	4.669	78.2°	0.117	69.4°	0.261	−35.6°
750.0	5	0.314	−173.9°	2.270	65.6°	0.153	59.1°	0.386	−40.7°
	20	0.194	175.0°	2.939	65.8°	0.182	64.7°	0.232	−30.4°
	40	0.180	172.2°	2.991	65.4°	0.186	65.7°	0.213	−27.1°
1000.0	5	0.287	168.8°	1.806	55.5°	0.193	59.8°	0.367	−54.1°
	20	0.172	162.3°	2.315	57.2°	0.233	61.2°	0.213	−44.1°
	40	0.156	158.7°	2.356	57.1°	0.238	61.4°	0.193	−41.6°
1250.0	5	0.283	147.5°	1.529	46.2°	0.233	59.2°	0.378	−60.0°
	20	0.164	138.4°	1.950	48.6°	0.279	57.2°	0.237	−46.7°
	40	0.152	134.6°	1.981	48.9°	0.283	56.8°	0.220	−44.5°
1500.0	5	0.297	131.8°	1.321	38.0°	0.272	58.4°	0.340	−71.1°
	20	0.171	124.3°	1.684	40.9°	0.317	53.3°	0.211	−52.8°
	40	0.160	120.6°	1.712	41.2°	0.325	53.1°	0.192	−48.6°



TYPICAL S_{11E} AND S_{22E} VS FREQUENCY

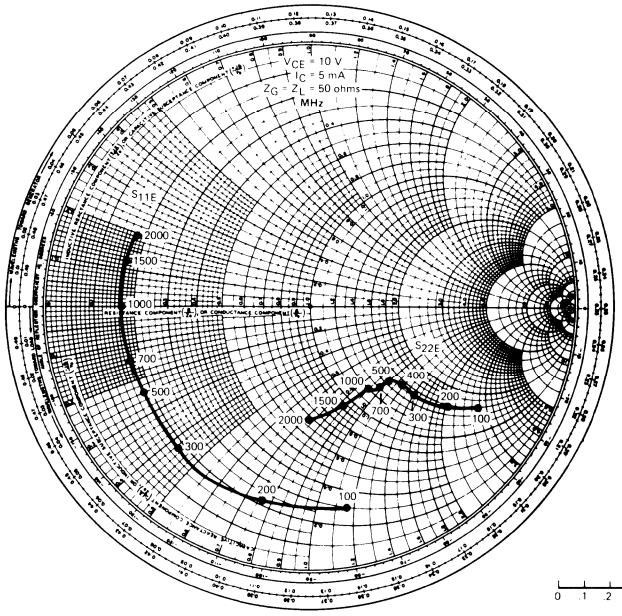


TYPICAL S_{12E} AND S_{21E} VS FREQUENCY

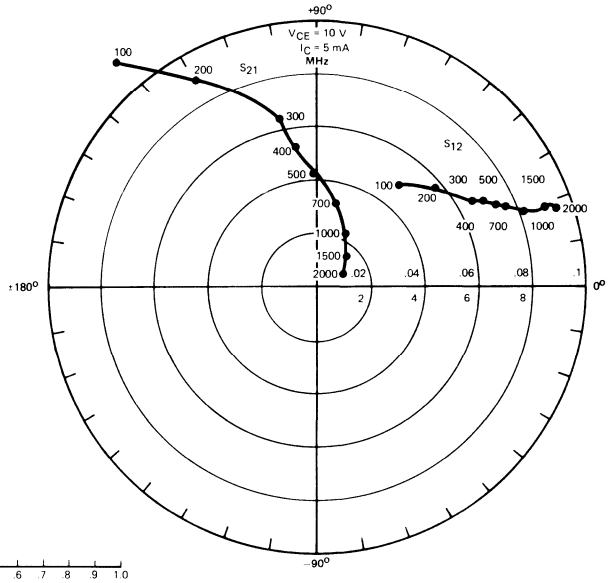
MA-42111-510
TYPICAL COMMON EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 10 VOLTS, $Z_G = Z_L = 50\ \Omega$

FREQUENCY (MHz)	COLLECTOR CURRENT (mA)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
		S_{11E}	ϕS_{11E}	S_{21E}	ϕS_{21E}	S_{12E}	ϕS_{12E}	S_{22E}	ϕS_{22E}
	5	0.734	− 77.8°	10.983	132.3°	0.049	48.4°	0.772	− 33.0°
110.0	20	0.501	−123.9°	20.284	112.0°	0.028	48.2°	0.468	− 59.1°
	40	0.476	−142.3°	23.431	110.1°	0.023	46.7°	0.416	− 74.5°
	5	0.688	−116.5°	7.607	110.5°	0.067	35.3°	0.573	− 42.6°
250.0	20	0.510	−152.6°	11.759	97.0°	0.040	53.7°	0.289	− 66.7°
	40	0.496	−164.3°	13.613	96.9°	0.033	46.9°	0.260	− 94.5°
	5	0.665	−155.0°	4.390	88.8°	0.078	26.0°	0.418	− 51.0°
500.0	20	0.520	−175.9°	6.123	80.0°	0.064	57.7°	0.173	− 72.3°
	40	0.517	−179.2°	7.079	81.0°	0.046	49.7°	0.165	−120.3°
	5	0.658	−174.4°	2.997	68.8°	0.080	23.1°	0.305	− 55.0°
750.0	20	0.488	170.4°	4.001	66.5°	0.087	58.8°	0.150	− 74.5°
	40	0.596	173.1°	4.754	67.9°	0.062	51.2°	0.138	−136.4°
	5	0.665	172.3°	2.307	55.4°	0.093	21.7°	0.361	− 62.4°
1000.0	20	0.505	160.6°	3.073	55.5°	0.122	56.5°	0.142	− 78.0°
	40	0.658	162.4°	3.636	58.3°	0.078	47.2°	0.131	−146.6°
	5	0.663	153.7°	1.509	33.8°	0.106	20.6°	0.355	− 81.8°
1500.0	20	0.437	142.5°	1.993	36.9°	0.220	50.1°	0.161	− 86.3°
	40	0.682	146.0°	2.288	41.1°	0.102	41.1°	0.141	−161.0°
	5	0.723	140.6°	1.147	14.3°	0.116	17.4°	0.398	−105.4°
2000.0	20	0.881	−132.8°	1.155	40.6°	0.957	−13.9°	0.630	−121.4°
	40	0.735	134.6°	1.784	25.0°	0.127	32.8°	0.172	−173.4°

specification sheet



TYPICAL S_{11E} AND S_{22E} VS FREQUENCY



TYPICAL S_{12E} AND S_{21E} VS FREQUENCY

MA-42111-511
TYPICAL COMMON EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 10 VOLTS, $Z_G = Z_L$ = 50 Ω

FREQUENCY (MHz)	COLLECTOR CURRENT (mA)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
		S_{11E}	ϕS_{11E}	S_{21E}	ϕS_{21E}	S_{12E}	ϕS_{12E}	S_{22E}	ϕS_{22E}
110.0	5	0.771	– 82.7°	11.479	134.8°	0.048	51.1°	0.761	– 38.0°
	20	0.651	–128.4°	22.742	115.5°	0.030	41.4°	0.493	– 69.3°
	40	0.629	–144.9°	25.899	109.3°	0.021	39.8°	0.400	– 83.1°
250.0	5	0.713	–115.5°	7.821	112.2°	0.064	36.1°	0.587	– 40.2°
	20	0.656	–150.4°	12.978	100.0°	0.034	38.9°	0.308	– 75.7°
	40	0.659	–159.9°	14.193	96.8°	0.028	45.4°	0.243	– 92.7°
500.0	5	0.692	–150.5°	4.359	90.0°	0.074	28.0°	0.430	– 45.9°
	20	0.667	–171.0°	6.547	84.4°	0.045	44.1°	0.179	– 87.2°
	40	0.666	–175.9°	7.196	83.4°	0.041	52.4°	0.148	113.3°
750.0	5	0.667	–168.5°	3.081	73.9°	0.076	22.5°	0.402	– 49.8°
	20	0.663	178.1°	4.738	73.7°	0.055	45.9°	0.142	– 94.7°
	40	0.664	174.6°	4.950	72.7°	0.052	54.0°	0.126	–123.8°
1000.0	5	0.696	–178.5°	2.322	62.2°	0.083	24.5°	0.382	– 55.8°
	20	0.689	171.2°	3.468	63.7°	0.069	45.8°	0.130	– 99.5°
	40	0.692	168.8°	3.689	64.3°	0.067	51.3°	0.115	–131.5°
1500.0	5	0.709	165.6°	1.592	42.6°	0.098	24.4°	0.389	– 72.2°
	20	0.687	169.3°	2.292	47.7°	0.092	44.7°	0.143	–112.2°
	40	0.693	157.8°	2.518	48.7°	0.091	49.4°	0.124	–140.8°
2000.0	5	0.720	155.0°	1.163	25.6°	0.103	25.6°	0.424	– 91.4°
	20	0.705	150.5°	1.703	33.4°	0.112	41.5°	0.172	–124.7°
	40	0.717	149.1°	1.836	35.2°	0.114	45.7°	0.157	–148.4°

specification sheet

npn silicon planar transistors

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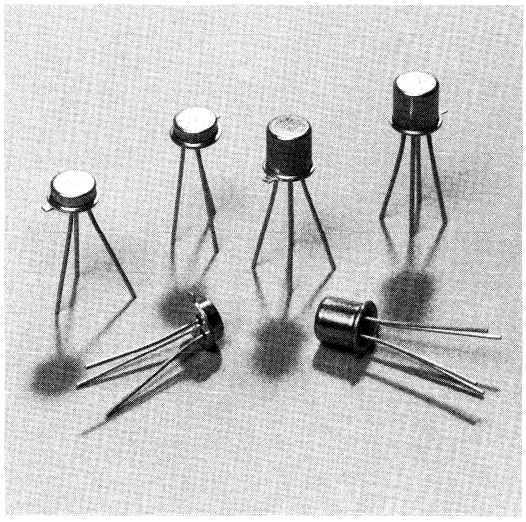
FEATURES

- HIGH GAIN BANDWIDTH PRODUCT (1.5 GHz)
- HIGH f_{max} (4.2 GHz @ I_C = 20 mA)
- GOLD METALLIZATION
- HIGH RELIABILITY
- DIRECT INTERCHANGABILITY WITH THE FMT 1060 SERIES OF FAIRCHILD TRANSISTORS

DESCRIPTION

This series of NPN Epitaxial Silicon Planar Transistors is designed for VHF/UHF service. The performance of this series is comparable to the Fairchild FMT-1060 series. The high gain bandwidth products make the MA-42122 and MA-42123 useful to 1.0 GHz while the MA-42120 and MA-42121 have a maximum frequency of oscillation of 4.0 GHz. Two packages are offered, the TO-46 (ODS-508), for low power oscillator applications and the TO-72 (ODS-509) for small signal UHF amplifiers.



APPLICATIONS

VHF, UHF Low Level Oscillators
IF and RF Amplifiers

MA-42120 SERIES R.F. SPECIFICATIONS

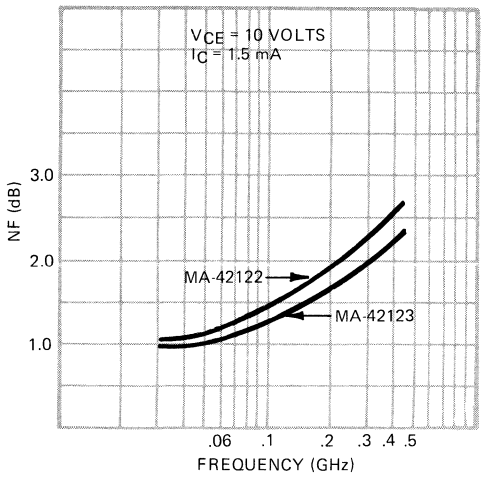
MODEL NO.	MA-42120	MA-42121	MA-42122	MA-42123
CASE STYLE	508	508	509	509
Test Frequency (MHz)	450	450	450	450
Max Noise Fig. @ I_C (dB)	– –	– –	3.5	3.0
Gu (max) Typ. (dB)	13	13	14	14
I_C (mA)	– –	– –	1.5	1.5
1 dB Compression Point (dBm)	– –	– –	–12	–12
Fairchild Equivalent	FMT 1060	FMT 1060A	FMT 1061	FMT 1061A

MA-42120 SERIES HIGH FREQUENCY SPECIFICATIONS (25°C Ambient Temperature Unless Otherwise Noted)

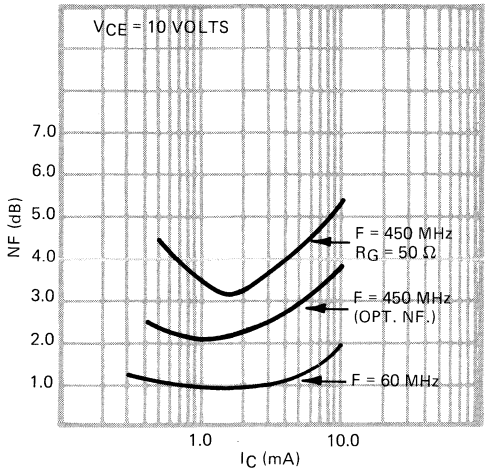
Symbol	Characteristics	Type	Min.	Typ.	Max.	Units	Test Conditions
f_t	Gain Bandwidth Product	MA42121	1.3	1.5		GHz	V_{CE} = 10V, I_C = 20 mA
		MA42120	1.0	1.3		GHz	f = 500 MHz
		MA42123	1.3	1.5		GHz	
		MA42122	1.0	1.3		GHz	
$G_{A\ max}$	Maximum Available Gain	MA42121		12.8		dB	V_{CE} = 10V, I_C = 20 mA
		MA42123		13.8			f = 1.0 GHz
NF	Noise Figure	MA42123		2.3	3.0	dB	V_{CE} = 10V, I_C = 1.5 mA
		MA42122		2.7	3.5	dB	f = 450 MHz, R = 50 ohms
G_{pe}	Neutralized Power Gain	MA42123		17.0		dB	V_{CE} = 10V, I_E = 1.5 mA
							f = 450 MHz, R = 50 ohms
f_{max}	Maximum Frequency of Oscillation[1]	MA42121		4.2		GHz	V_{CE} = 10V, I_C = 20 mA
		MA42120		3.8		GHz	V_{CE} = 10V, I_C = 20 mA

NOTE:

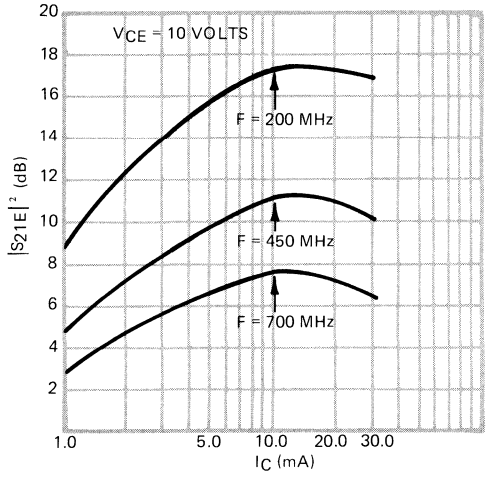
1. Calculated from S-Parameters, f_{max} is the frequency at which the extrapolated GA_{max} is 0 dB.



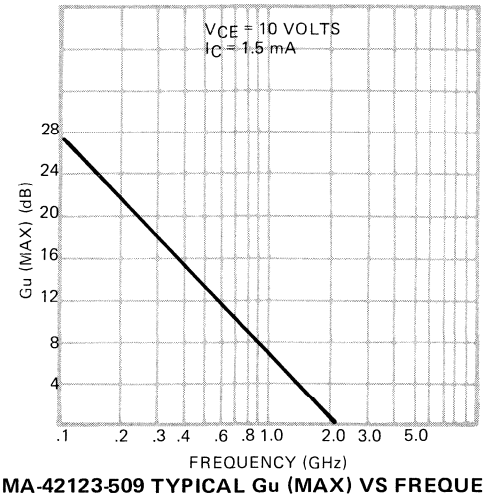
TYPICAL NOISE FIGURE VS FREQUENCY



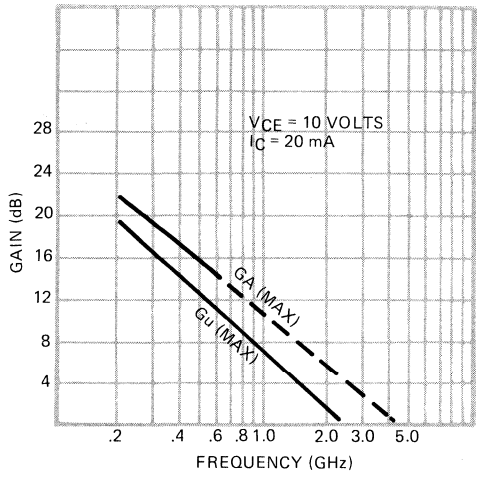
MA-42123-509 TYPICAL OPTIMUM N.F. VS COLLECTOR CURRENT



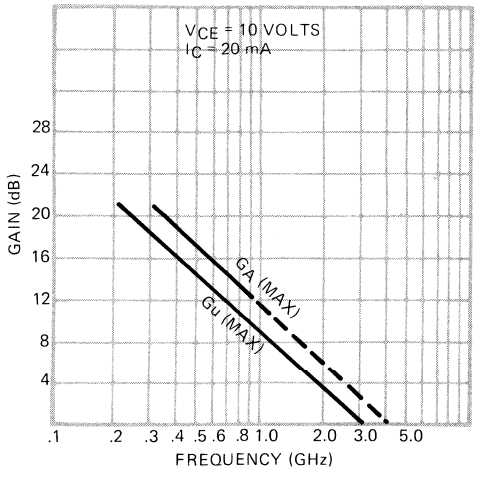
MA-42123-509 TYPICAL $|S_{21E}|^2$ VS COLLECTOR CURRENT



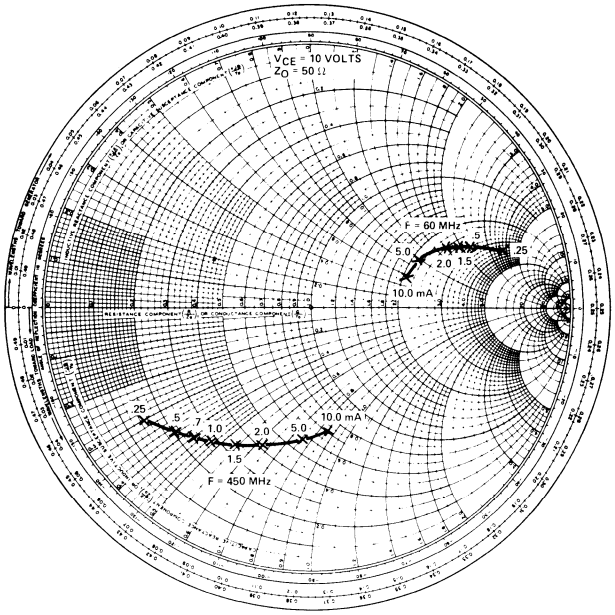
MA-42123-509 TYPICAL Gu (MAX) VS FREQUENCY



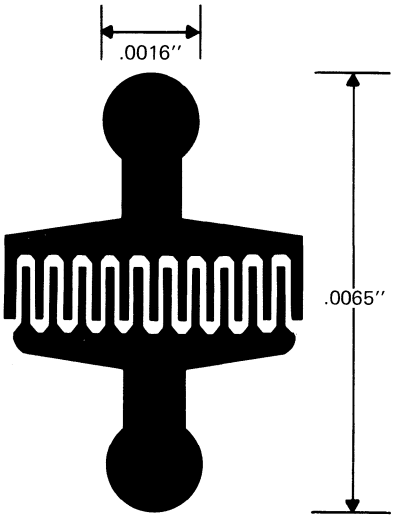
MA-42120-508 TYPICAL GAIN VS FREQUENCY



MA-42121-508 TYPICAL GAIN VS FREQUENCY



TYPICAL OPTIMUM NOISE SOURCE IMPEDANCE VS COLLECTOR CURRENT



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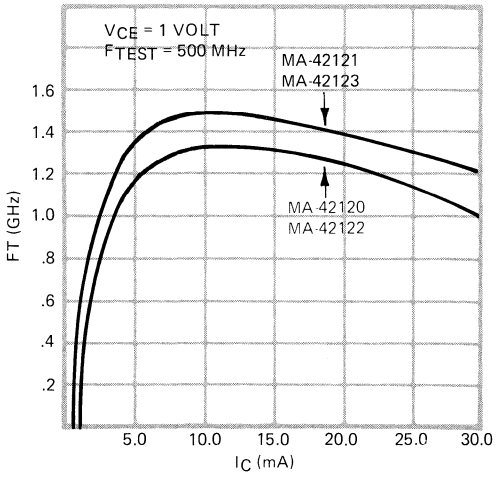
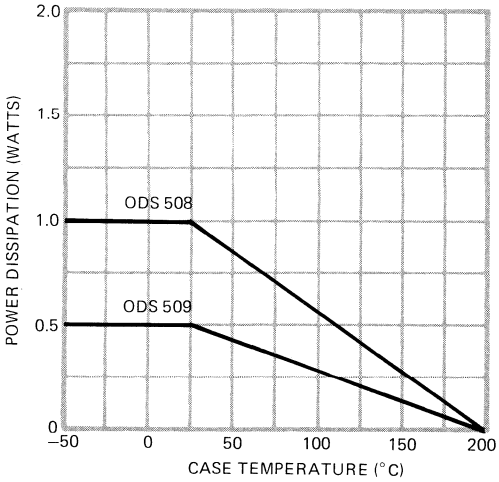


MA-42120 SERIES TYPICAL F_T VS COLLECTOR CURRENT



MA-42120 SERIES POWER DISSIPATION VS. CASE TEMPERATURE

specification sheet

ELECTRICAL CHARACTERISTICS (25°C Ambient Temperature Unless Otherwise Noted)

Symbol	Characteristics	MA42120 MA42122 Min	Typ	Max	MA42121 MA42123 Min	Typ	Max	Units	Test Conditions
h_{FE}	DC Current Gain	20	45	110	40	75	185		I_C = 5.0 mA, V_{CE} = 5.0
V_{CE} (sat)	Pulsed Collector Saturation Voltage[1]		0.30	0.38		0.25	0.35	V	I_C = 80 mA, I_B = 8.0 mA
V_{BE} (sat)	Pulsed Base Saturation Voltage[1]		0.95	0.98		0.93	0.96	V	I_C = 40 mA, I_B = 20 mA
BV_{CBO}	Collector to Base Breakdown	30	35		30	35		V	I_C = 10 μA, I_E = 0
V_{CEO} (sus)	Collector to Emitter Sustaining Voltage	14	16.5		14	16.5		V	I_C = 1.0 mA, I_B = 0
I_{EBO}	Emitter Cutoff Current		20	100		20	100	μA	I_C = 0, V_{EB} = 4.0V
I_{CBO}	Collector Cutoff Current		0.01	50		0.01	50	nA	V_{CB} = 10V, I_E = 0
I_{CBO}	Collector Cutoff Current		0.3	1.0		0.3	1.0	μA	V_{CB} = 10V, I_E = 0 T_A = 125°C
C_{cb}	Collector to Base Capacitance (MA42120, MA42121)		1.0	1.4		1.0	1.4	pF	V_{CB} = 10V, I_E = 0
C_{cb}	Collector to Base Capacitance (MA42122, MA42123)		0.85	1.0		0.85	1.0	pF	V_{CB} = 10V, I_E = 0
C_{eb}	Emitter to Base Capacitance		1.5	3.0		1.5	3.0	pF	V_{EB} = 0.5V, I_C = 0
$\|h_{fe}\|$	Magnitude of High Frequency Current Gain	2.0	2.6		2.6	3.0			V_{CE} = 10V, I_C = 20 mA, f = 500 MHz

NOTE:

1. Pulse Conditions: Length = 300 μs; duty cycle = 1%

MAXIMUM RATING
(Case Temperature 25°C unless otherwise noted)

	Total Power Dissipation	508 case — 1.0 W 509 case — .5 W
V_{CBO}	**Collector to Base Voltage**	30 V
V_{EBO}	**Emitter to Base Voltage**	4.0 V
V_{CES}	**Collector to Emitter Voltage**	30 V
I_C	**Collector Current**	80 mA
	Storage Temperature	−65° to +200°C
	Operating Junction Temperature	+200°C
	Lead Temperature (Soldering — 10 seconds each lead)	+250°C
	Hermeticity	$5 \times (10)^{-8}$ cc/sec of He

ENVIRONMENTAL RATINGS PER MIL-STD-750

	Method	Level
Storage Temperature	1031	−65 to +200°C
Temperature Cycle	1051	10 cycles −65 to +200°C
Shock	2016	500 g's
Vibration	2056	15 g's
Constant Acceleration	2006	20,000 g's
Humidity	1021	10 days

MA-42120-508
TYPICAL COMMON-EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 10 VOLTS, $Z_G = Z_L = 50\ \Omega$

FREQUENCY (MHz)	COLLECTOR CURRENT (mA)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
		$\lvert S_{11E}\rvert$	ϕS_{11E}	$\lvert S_{21E}\rvert$	ϕS_{21E}	$\lvert S_{12E}\rvert$	ϕS_{12E}	$\lvert S_{22E}\rvert$	ϕS_{22E}
100	1.5	.89	−44°	3.8	146°	.05	65°	.94	−13°
	5.0	.69	−79°	8.6	126°	.03	55°	.81	−18°
	20.0	.50	−127°	12.0	107°	.02	52°	.67	−16°
200	1.5	.80	−72°	3.3	128°	.06	51°	.86	−20°
	5.0	.60	−113°	6.1	107°	.04	49°	.71	−21°
	20.0	.50	−150°	7.4	92°	.02	62°	.61	−16°
300	1.5	.72	−95°	2.7	112°	.07	43°	.82	−25°
	5.0	.55	−134°	4.3	95°	.04	50°	.68	−23°
	20.0	.51	−161°	5.0	83°	.03	68°	.61	−18°
400	1.5	.66	−115°	2.2	101°	.08	38°	.79	−29°
	5.0	.53	−148°	3.4	86°	.05	54°	.66	−25°
	20.0	.52	−169°	3.8	75°	.04	72°	.62	−20°
450	1.5	.64	−123°	2.1	95°	.07	38°	.77	−30°
	5.0	.53	−154°	3.1	81°	.05	58°	.66	−27°
	20.0	.53	−172°	3.4	71°	.04	77°	.63	−21°
500	1.5	.63	−130°	1.9	90°	.07	39°	.76	−32°
	5.0	.53	−159°	2.7	77°	.05	62°	.66	−28°
	20.0	.54	−175°	3.0	67°	.05	79°	.63	−23°
600	1.5	.61	−143°	1.6	83°	.07	40°	.73	−35°
	5.0	.53	−167°	2.3	72°	.06	66°	.65	−31°
	20.0	.55	178°	2.5	63°	.06	82°	.63	−26°
700	1.5	.61	−153°	1.5	76°	.07	46°	.70	−39°
	5.0	.55	−174°	2.0	65°	.06	74°	.63	−34°
	20.0	.57	174°	2.2	56°	.06	87°	.62	−29°
800	1.5	.61	−162°	1.3	70°	.06	55°	.68	−44°
	5.0	.56	179°	1.8	61°	.07	79°	.62	−38°
	20.0	.59	170°	1.8	52°	.08	91°	.62	−34°
900	1.5	.61	−169°	1.2	66°	.07	64°	.68	−50°
	5.0	.56	174°	1.6	57°	.08	84°	.62	−44°
	20.0	.60	166°	1.6	49°	.09	94°	.62	−41°
1000	1.5	.61	−176°	1.1	60°	.07	77°	.68	−55°
	5.0	.56	169°	1.4	52°	.09	91°	.63	−50°
	20.0	.61	160°	1.5	44°	.10	99°	.63	−47°

MA 42121-508
TYPICAL COMMON-EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 10 VOLTS, $Z_G = Z_L = 50$

FREQUENCY (MHz)	COLLECTOR CURRENT (mA)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
		$\lvert S_{11E}\rvert$	ϕS_{11E}	$\lvert S_{21E}\rvert$	ϕS_{21E}	$\lvert S_{12E}\rvert$	ϕS_{12E}	$\lvert S_{22E}\rvert$	ϕS_{22E}
100	1.5	.92	−36°	3.8	150°	.04	67°	.95	−13°
	5.0	.74	−67°	9.1	131°	.03	59°	.82	−19°
	20.0	.51	−118°	13	109°	.02	55°	.66	−18°
200	1.5	.83	−59°	3.4	133°	.07	55°	.86	−21°
	5.0	.61	−98°	6.7	111°	.04	48°	.69	−24°
	20.0	.49	−142°	8.0	93°	.03	59°	.59	−18°
300	1.5	.74	−81°	2.9	117°	.08	47°	.81	−27°
	5.0	.54	−120°	4.9	99°	.05	50°	.65	−26°
	20.0	.49	−156°	5.5	84°	.03	65°	.58	−19°
400	1.5	.67	−99°	2.5	106°	.09	41°	.77	−31°
	5.0	.51	−136°	3.9	89°	.06	51°	.62	−28°
	20.0	.50	−164°	4.2	77°	.04	67°	.59	−22°
450	1.5	.65	−106°	2.3	100°	.09	40°	.75	−33°
	5.0	.50	−142°	3.5	85°	.06	53°	.62	−29°
	20.0	.51	−167°	3.7	73°	.05	71°	.59	−23°
500	1.5	.62	−114°	2.1	95°	.09	40°	.74	−35°
	5.0	.50	−147°	3.1	81°	.06	55°	.62	−30°
	20.0	.51	−170°	3.3	69°	.05	74°	.60	−24°
600	1.5	.59	−127°	1.8	88°	.09	38°	.71	−37°
	5.0	.49	−157°	2.6	75°	.06	58°	.61	−32°
	20.0	.53	−176°	2.7	64°	.06	76°	.60	−26°
700	1.5	.58	−138°	1.6	80°	.09	39°	.68	−41°
	5.0	.50	−164°	2.3	68°	.07	63°	.59	−35°
	20.0	.55	179°	2.4	58°	.06	81°	.59	−30°
800	1.5	.58	−147°	1.5	74°	.08	43°	.65	−45°
	5.0	.51	−170°	2.0	63°	.08	68°	.57	−39°
	20.0	.57	175°	2.0	54°	.07	84°	.59	−35°
900	1.5	.58	−154°	1.3	69°	.08	47°	.65	−51°
	5.0	.52	−174°	1.8	60°	.08	71°	.57	−44°
	20.0	.58	171°	1.8	51°	.08	88°	.59	−41°
1000	1.5	.57	−161°	1.2	64°	.08	56°	.65	−56°
	5.0	.52	−179°	1.6	55°	.09	78°	.59	−49°
	20.0	.59	166°	1.6	46°	.09	93°	.61	−46°

specification sheet

MA 42122-509
TYPICAL COMMON-EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 10 VOLTS, $Z_G = Z_L = 50\ \Omega$

FREQUENCY (MHz)	COLLECTOR CURRENT (mA)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
		$\lvert S_{11E} \rvert$	ϕS_{11E}	$\lvert S_{21E} \rvert$	ϕS_{21E}	$\lvert S_{12E} \rvert$	ϕS_{12E}	$\lvert S_{22E} \rvert$	ϕS_{22E}
100	1.5	.87	−43°	3.7	145°	.03	63°	.96	−10°
	5.0	.66	−70°	8.1	127°	.02	53°	.87	−12°
	20.0	.43	−103°	11.2	109°	.02	55°	.78	−12°
200	1.5	.76	−69°	3.2	127°	.04	54°	.89	−15°
	5.0	.52	−102°	5.7	107°	.03	56°	.79	−16°
	20.0	.37	−132°	7.0	93°	.02	66°	.73	−13°
300	1.5	.66	−94°	2.6	110°	.05	47°	.86	−19°
	5.0	.45	−126°	4.1	94°	.03	58°	.77	−18°
	20.0	.36	−149°	4.8	83°	.03	70°	.73	−15°
400	1.5	.69	−115°	2.2	99°	.05	45°	.84	−23°
	5.0	.41	−144°	3.3	84°	.04	62°	.76	−21°
	20.0	.37	−162°	3.7	75°	.04	73°	.73	−17°
450	1.5	.56	−124°	2.0	93°	.05	47°	.83	−25°
	5.0	.40	−151°	2.9	79°	.04	66°	.76	−22°
	20.0	.37	−167°	3.3	70°	.04	76°	.73	−19°
500	1.5	.54	−132°	1.8	88°	.05	49°	.82	−26°
	5.0	.40	−157°	2.6	75°	.05	69°	.75	−23°
	20.0	.37	−172°	2.9	66°	.05	79°	.73	−21°
600	1.5	.61	−148°	1.6	80°	.05	53°	.80	−29°
	5.0	.40	−169°	2.2	69°	.05	74°	.74	−26°
	20.0	.39	179°	2.4	60°	.06	81°	.73	−23°
700	1.5	.50	−160°	1.4	72°	.05	63°	.77	−33°
	5.0	.40	−179°	2.0	62°	.06	79°	.72	−29°
	20.0	.41	172°	2.1	53°	.06	84°	.72	−27°
800	1.5	.50	−171°	1.3	66°	.08	72°	.74	−38°
	5.0	.41	173°	1.7	57°	.07	83°	.71	−34°
	20.0	.43	166°	1.8	49°	.08	87°	.70	−32°
900	1.5	.49	178°	1.2	61°	.07	80°	.74	−43°
	5.0	.41	166°	1.6	52°	.08	85°	.70	−39°
	20.0	.43	159°	1.6	45°	.09	88°	.70	−37°
1000	1.5	.48	168°	1.1	55°	.08	89°	.74	−48°
	5.0	.41	167°	1.4	47°	.10	90°	.71	−45°
	20.0	.44	151°	1.5	39°	.11	93°	.70	−42°

MA 42123-509
TYPICAL COMMON-EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 10 VOLTS, $Z_G = Z_L = 50\ \Omega$

FREQUENCY (MHz)	COLLECTOR CURRENT (mA)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
		$\lvert S_{11E} \rvert$	ϕS_{11E}	$\lvert S_{21E} \rvert$	ϕS_{21E}	$\lvert S_{12E} \rvert$	ϕS_{12E}	$\lvert S_{22E} \rvert$	ϕS_{22E}
100	1.5	.89	−39°	3.8	147°	.04	54°	.95	−11°
	5.0	.68	−85°	8.6	128°	.03	56°	.85	−15°
	20.0	.43	−121°	10.9	104°	.02	57°	.67	−16°
200	1.5	.79	−63°	3.3	129°	.05	56°	.87	−17°
	5.0	.53	−95°	6.1	108°	.04	55°	.75	−17°
	20.0	.40	−144°	6.6	89°	.03	66°	.61	−16°
300	1.5	.69	−86°	2.7	113°	.06	48°	.84	−21°
	5.0	.45	−118°	4.4	95°	.05	57°	.72	−20°
	20.0	.41	−158°	4.5	80°	.04	70°	.61	−18°
400	1.5	.61	−105°	2.3	101°	.07	44°	.81	−25°
	5.0	.41	−135°	3.5	86°	.05	58°	.71	−22°
	20.0	.41	−168°	3.5	72°	.06	72°	.61	−21°
450	1.5	.58	−114°	2.2	96°	.07	45°	.79	−27°
	5.0	.40	−141°	3.2	81°	.05	62°	.70	−23°
	20.0	.42	−172°	3.1	67°	.06	73°	.61	−22°
500	1.5	.55	−121°	2.0	91°	.07	45°	.79	−28°
	5.0	.39	−148°	2.8	77°	.06	65°	.70	−24°
	20.0	.43	−176°	2.7	64°	.07	76°	.62	−24°
600	1.5	.52	−136°	1.7	83°	.07	46°	.76	−31°
	5.0	.39	−159°	2.4	71°	.06	66°	.69	−27°
	20.0	.45	177°	2.3	58°	.08	77°	.62	−27°
700	1.5	.50	−148°	1.6	74°	.07	51°	.73	−34°
	5.0	.39	−168°	2.1	64°	.07	70°	.67	−29°
	20.0	.47	171°	2.0	51°	.09	80°	.61	−31°
800	1.5	.50	−159°	1.4	68°	.07	57°	.71	−39°
	5.0	.39	−176°	1.9	59°	.08	74°	.66	−33°
	20.0	.48	166°	1.7	47°	.11	83°	.60	−36°
900	1.5	.49	−167°	1.3	63°	.07	64°	.70	−43°
	5.0	.39	178°	1.7	55°	.09	76°	.65	−38°
	20.0	.49	160°	1.5	43°	.12	84°	.59	−43°
1000	1.5	.47	−176°	1.2	57°	.08	74°	.70	−49°
	5.0	.39	171°	1.5	49°	.10	81°	.66	−43°
	20.0	.50	154°	1.4	37°	.14	87°	.60	−49°

specification sheet

npn silicon planar transistors

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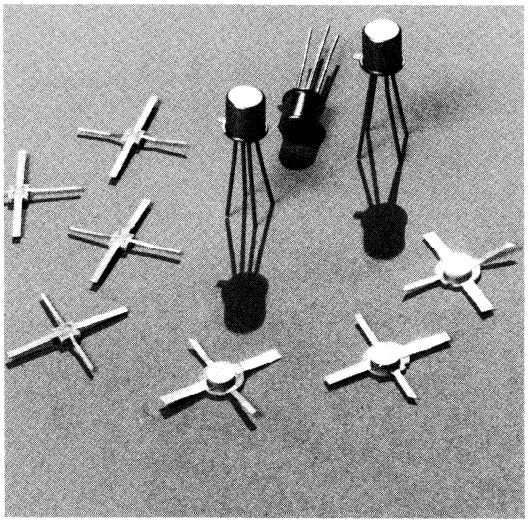
FEATURES

- LOW INTRINSIC NOISE FIGURE AT 1.0 GHz – 2.3 dB TYPICAL
- HIGH POWER GAIN AT 1.0 GHz – 18.0 dB TYPICAL
- ION IMPLANTED ARSENIC EMITTER FOR CONSISTENT PERFORMANCE
- GOLD METALLIZATION
- HIGH RELIABILITY

DESCRIPTION

This series of npn silicon planar transistors finds application in low noise and medium power microwave amplifier circuitry. The MA-42141 exhibits an excellent noise figure characteristic over the frequency range of .5 to 2 GHz. The performance of this transistor is comparable to the Fairchild FMT-4225. These units feature good high frequency current gain at medium current levels.



APPLICATIONS

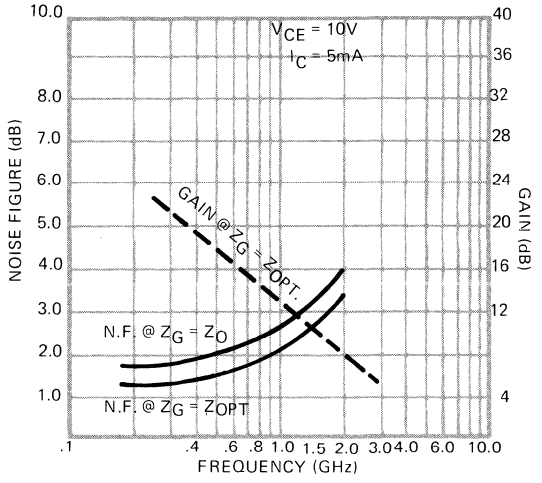
RF Amplifiers
Low Level Oscillators

MA-42140 SERIES R.F. SPECIFICATIONS

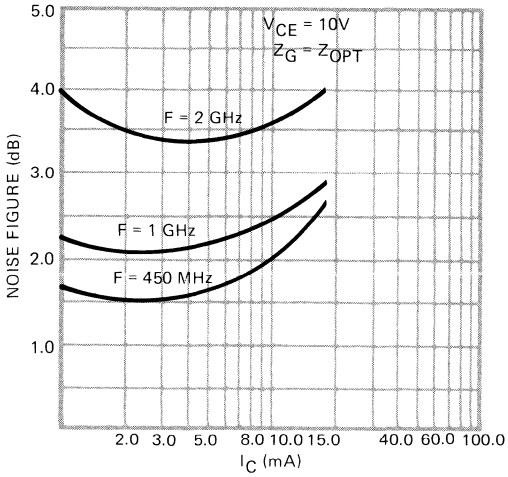
MODEL NO.	MA-42141	MA-42142	MA-42143	2N5651	2N5652
CASE STYLE	509/510/511	509/510/511	509/510/511	509	509
Test Frequency (GHz)	1	1	450	450	450
Max Noise Fig. @ I_C (dB)	2.5	3.0	1.7	2.0	2.5
G_U (max) Typ (dB)	17	17	18	21	21
I_C (mA)	15	15	15	15	15
1 dB Compression Point (dBm) @ I_C	+10	+10	+10	+11	+11

ELECTRICAL CHARACTERISTICS (Case temperature 25°C)

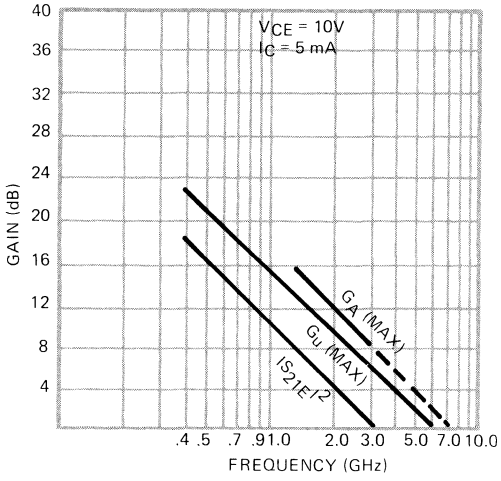
Symbol	Definition	Conditions	Min.	Typ.	Max.
BV_{CBO}	Collector-base breakdown voltage	I_C = 10 μA	27V	35V	
BV_{EBO}	Emitter-base breakdown voltage	I_E = 10 μA	3V	3.5V	
BV_{CEO}	Collector-Emitter breakdown Voltage	I_C = 500 μA	20V	25V	
I_{CBO}	Collector-cut-off current	V_{CB} = 10 V			100 nA
h_{FE}	Current transfer ratio	V_{CE} = 10 V, I_C = 5 mA	20		200
C_{CB}	Output Capacitance	V_{CB} = 15 V			1.0 pF



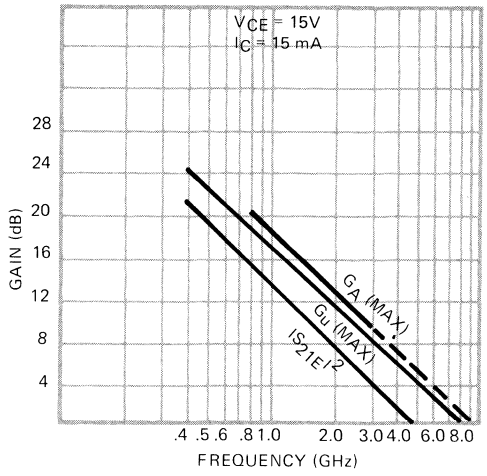
TYPICAL NOISE FIGURE AND ASSOCIATED GAIN VS FREQUENCY



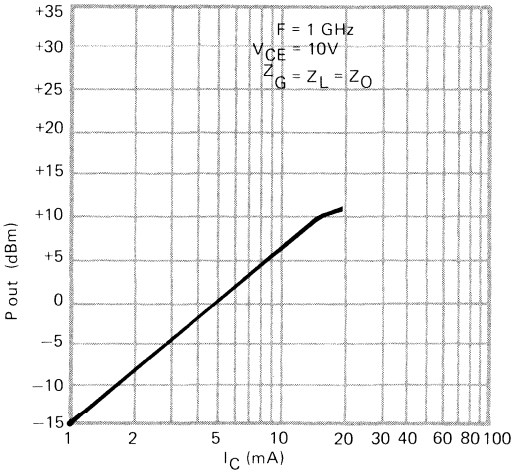
TYPICAL NOISE FIGURE VS COLLECTOR CURRENT



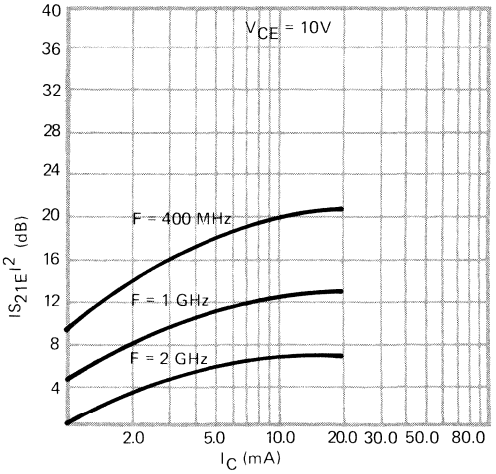
TYPICAL GAIN PARAMETERS VS FREQUENCY



TYPICAL GAIN PARAMETERS VS FREQUENCY

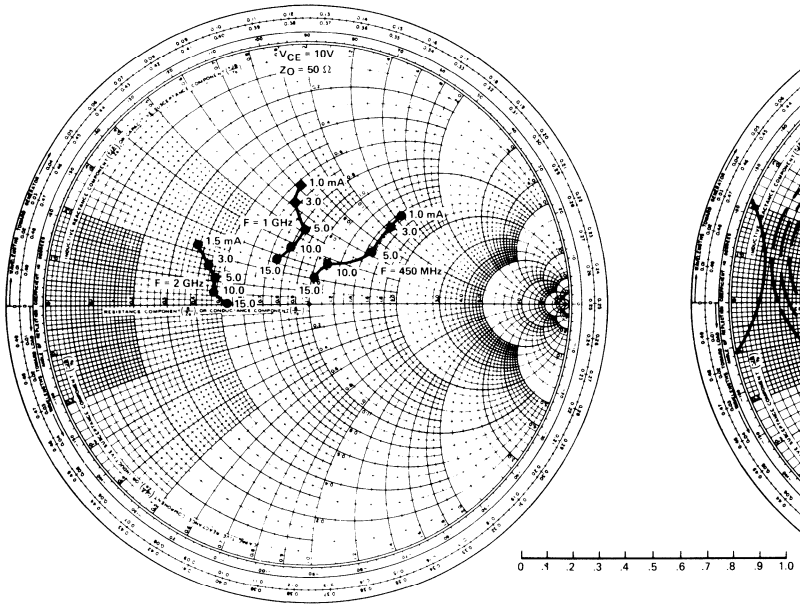


TYPICAL POWER OUTPUT AT 1 dB COMPRESSION VS COLLECTOR CURRENT

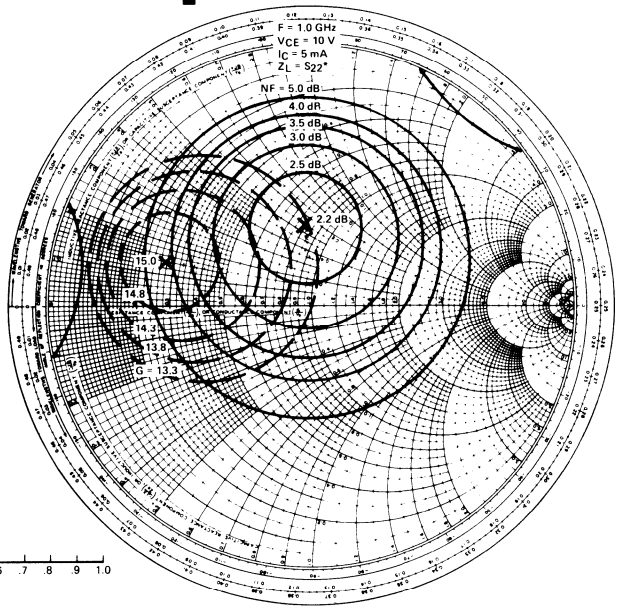


TYPICAL $|S_{21E}|^2$ VS COLLECTOR CURRENT

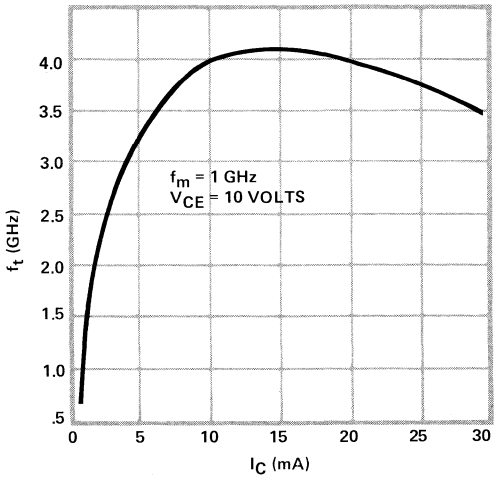
specification sheet



TYPICAL OPTIMUM NOISE SOURCE IMPEDANCE VS COLLECTOR CURRENT AND FREQUENCY



TYPICAL CONSTANT GAIN AND N.F. CIRCLES



TYPICAL f_t VS COLLECTOR CURRENT

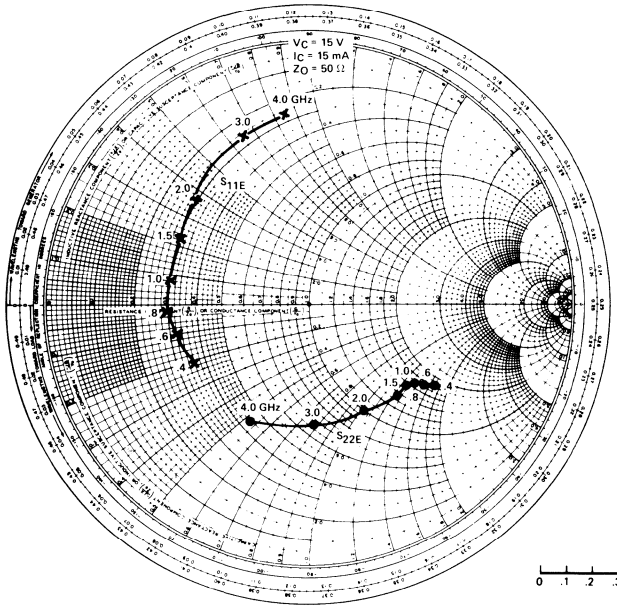
MAXIMUM RATING
(Case Temperature 25°C unless otherwise noted)

Total Device Power Dissipation	509 Case – 400mW 510 Case – 700 mW 511 Case – 700 mW
V_{CBO} Collector to Base Voltage	27 V
V_{EBO} Emitter to Base Voltage	3 V
I_C Collector Current	50 mA
Storage Temperature	–65 to +200°C
Operating Junction Temperature	+200°C
Hermeticity	5 x $(10)^{-8}$ cc/sec of He
Lead Temperature (Soldering – 10 seconds each lead)	250°C

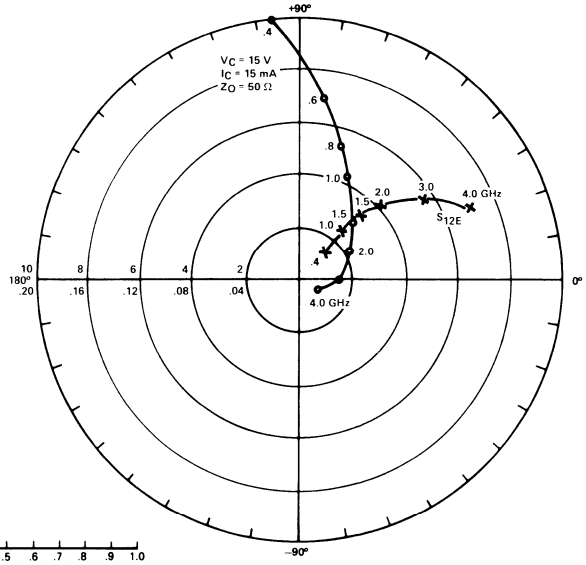
ENVIRONMENTAL RATINGS PER MIL-STD-750

	Method	Level
Storage Temperature	1031	–65 to +200°C
Temperature Cycle	1051	10 cycles –65 to +200°C
Shock	2016	500 g's
Vibration	2056	15 g's
Constant Acceleration	2006	20,000 g's
Humidity	1021	10 days

specification sheet



TYPICAL S_{11E} AND S_{22E} VS FREQUENCY



TYPICAL S_{21E} AND S_{12E} VS FREQUENCY

MA-42141-510
TYPICAL COMMON-EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 15 VOLTS, I_C = 15 mA, $Z_G = Z_L$ = 50 Ω

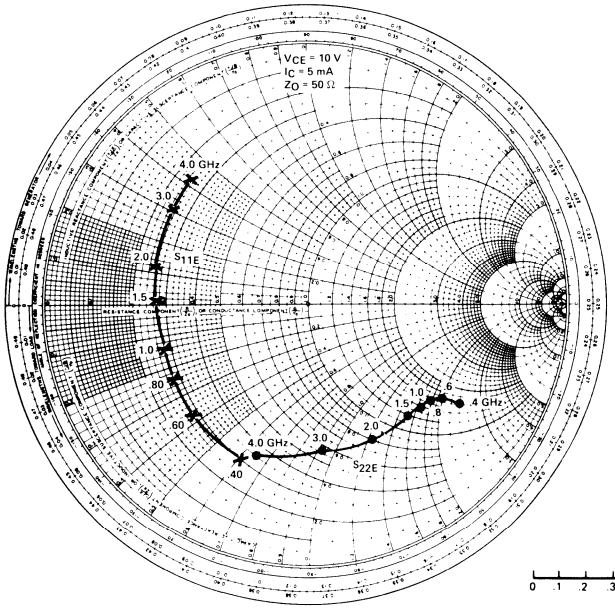
FREQUENCY (MHz)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
	S_{11E}	ϕS_{11E}	S_{21E}	ϕS_{21E}	S_{12E}	ϕS_{12E}	S_{22E}	ϕS_{22E}
400.0	.503	−150.9°	9.982	96.3°	.038	46.7°	.574	−34.0°
500.0	.511	−159.8°	8.190	88.6°	.033	47.1°	.530	−33.0°
800.0	.512	179.4°	5.323	72.8°	.043	49.2°	.519	−37.7°
1200.0	.523	162.1°	3.655	57.3°	.057	48.2°	.490	−42.5°
1600.0	.542	147.2°	2.781	42.5°	.070	46.0°	.498	−50.8°
2000.0	.577	136.2°	2.251	31.2°	.083	43.3°	.493	−64.0°
2400.0	.612	125.3°	1.698	17.3°	.094	39.1°	.488	−71.9°
2800.0	.634	115.1°	1.656	3.9°	.107	34.0°	.479	−84.0°
3200.0	.681	106.8°	1.419	− 8.1°	.119	30.1°	.494	−95.4°
3600.0	.705	97.8°	1.257	−20.5°	.130	26.1°	.498	−109.2°
4000.0	.709	96.7°	1.107	−21.9°	.142	28.1°	.605	−116.6°
4400.0	.725	89.5°	.973	−34.1°	.159	20.9°	.541	−131.8°
4800.0	.733	82.7°	.857	−45.8°	.170	14.8°	.582	−147.3°
5000.0	.732	78.7°	.804	−51.5°	.178	12.6°	.590	−155.2°

MA-42141-510
TYPICAL COMMON-EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 10 VOLTS, I_C = 5 mA, $Z_G = Z_L$ = 50 Ω

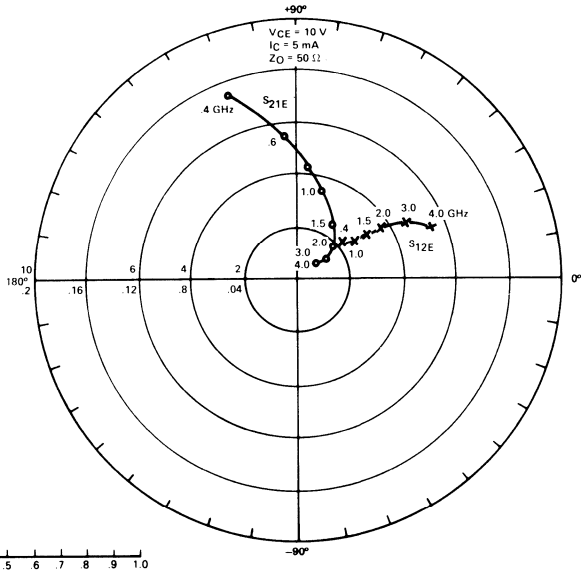
FREQUENCY (MHz)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
	S_{11E}	ϕS_{11E}	S_{21E}	ϕS_{21E}	S_{12E}	ϕS_{12E}	S_{22E}	ϕS_{22E}
400.0	.597	−118.5°	7.339	105.5°	.050	40.5°	.693	−37.5°
500.0	.579	−132.2°	6.284	96.5°	.052	37.6°	.622	−37.4°
800.0	.544	−161.5°	4.174	77.7°	.061	33.6°	.574	−43.6°
1200.0	.536	−174.6°	2.932	56.3°	.071	31.2°	.533	−48.9°
1600.0	.544	156.1°	2.235	42.1°	.081	29.6°	.537	−57.4°
2000.0	.577	142.8°	1.810	29.9°	.093	29.5°	.526	−71.1°
2400.0	.609	130.2°	1.537	15.1°	.102	26.4°	.523	−79.8°
2800.0	.630	118.6°	1.338	− .1°	.113	22.2°	.513	−93.0°
3200.0	.670	109.8°	1.141	−12.6°	.122	19.3°	.530	−104.7°
3600.0	.708	108.6°	1.017	−25.3°	.134	15.9°	.545	−110.7°
4000.0	.697	98.9°	.876	−27.6°	.143	18.0°	.545	−127.1°
4400.0	.711	91.5°	.756	−40.0°	.108	12.0°	.588	−141.8°
4800.0	.722	84.7°	.659	−51.3°	.167	5.9°	.633	−157.6°
5000.0	.718	81.0°	.614	−56.4°	.173	3.9°	.636	−165.5°

NOTE:
S-Parameter measurements taken using a WATS type 7025 Transistor test fixture. Input power level less than −25 dBm.

specification sheet



TYPICAL S_{11E} AND S_{22E} VS FREQUENCY



TYPICAL S_{12E} AND S_{21E} VS FREQUENCY

MA-42141-511
TYPICAL COMMON-EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 10 VOLTS, I_C = 5 mA, $Z_G = Z_L$ = 50 Ω

FREQUENCY (MHz)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
	S_{11E}	ϕS_{11E}	S_{21E}	ϕS_{21E}	S_{12E}	ϕS_{12E}	S_{22E}	ϕS_{22E}
400.0	.626	−112.9°	7.563	110.3°	.044	43.0°	.726	−34.3°
500.0	.618	−125.0°	6.425	102.1°	.046	38.9°	.660	−32.9°
800.0	.577	−150.8°	4.363	84.7°	.054	34.3°	.616	−38.6°
1200.0	.566	−170.1°	3.073	67.7°	.062	32.9°	.577	−43.1°
1600.0	.661	−175.9°	2.344	54.1°	.069	32.6°	.578	−50.4°
2000.0	.561	166.2°	1.894	43.2°	.078	32.6°	.571	−63.6°
2400.0	.597	156.6°	1.608	30.6°	.084	30.3°	.572	−70.8°
2800.0	.506	147.8°	1.408	17.9°	.093	27.0°	.565	−81.4°
3200.0	.630	141.1°	1.200	6.8°	.099	24.6°	.583	−90.7°
3600.0	.651	133.7°	1.072	−4.6°	.106	21.7°	.597	−102.6°
4000.0	.643	132.9°	.933	−6.5°	.109	24.7°	.599	−109.2°
4400.0	.643	127.7°	.796	−18.4°	.112	21.4°	.637	−121.6°
4800.0	.656	122.7°	.702	−28.8°	.123	17.0°	.686	−135.2°
5000.0	.652	120.1°	.657	−34.1°	.123	14.0°	.693	−142.1°

MA-42141-511
TYPICAL COMMON–EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 15 VOLTS, I_C = 15 mA, $Z_G = Z_L$ = 50 Ω

FREQUENCY (MHz)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
	S_{11E}	ϕS_{11E}	S_{21E}	ϕS_{21E}	S_{12E}	ϕS_{12E}	S_{22E}	ϕS_{22E}
400.0	.537	−143.2°	10.294	100.9°	.026	45.4°	.608	− 31.2°
500.0	.547	−152.2°	8.564	93.7°	.028	46.0°	.569	− 29.3°
800.0	.548	−170.2°	5.694	79.2°	.036	47.2°	.562	− 33.5°
1200.0	.550	−176.9°	3.867	65.9°	.046	48.7°	.532	− 37.3°
1600.0	.562	166.4°	2.946	53.6°	.056	48.0°	.539	− 43.9°
2000.0	.579	158.8°	2.383	43.8°	.067	47.2°	.539	− 56.9°
2400.0	.601	150.8°	2.010	32.1°	.074	43.4°	.537	− 63.4°
2800.0	.608	143.3°	1.755	20.0°	.083	39.7°	.530	− 73.5°
3200.0	.643	137.0°	1.505	10.4°	.091	36.6°	.553	− 82.5°
3600.0	.657	130.1°	1.338	− .0°	.098	33.5°	.560	− 94.1°
4000.0	.654	129.7°	1.188	− 1.4°	.104	36.2°	.565	− 99.8°
4400.0	.648	124.6°	1.017	− 13.3°	.107	32.5°	.600	−112.7°
4800.0	.665	120.1°	.905	− 23.4°	.120	27.5°	.648	−125.9°
5000.0	.650	117.2°	.849	− 28.9°	.121	24.4°	.657	−133.0°

NOTE:
S-Parameter measurements taken using a WATS type 7025 Transistor Text Fixture. Input power level less than −25 dBm.

MA-42140 SERIES

specification sheet

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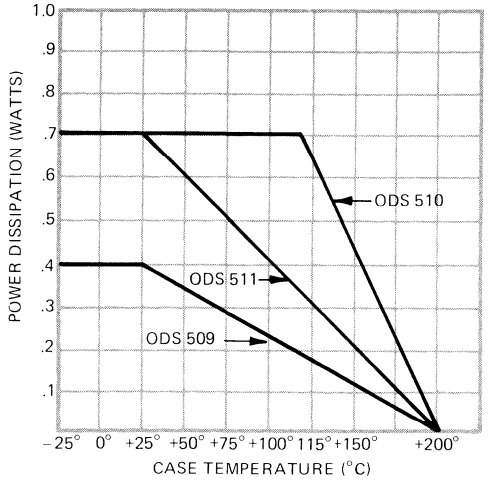
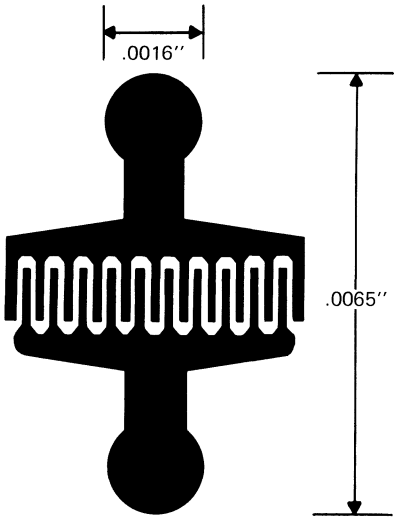


POWER DISSIPATION VS CASE TEMPERATURE



GEOMETRY 63

MA-42140 SERIES R.F. SPECIFICATIONS

Symbol	Definition	Conditions	Min.	Typ.	Max.	Units	Model
NF	Noise Figure	V_{CE} = 10V, I_C = 5 mA	– –	– –	2.5	dB	MA-42141
		1 GHz			3.0	dB	MA-42142
		V_{CE} = 10V, I_C = 1.5 mA .45 GHz	– –	– –	1.7	dB	MA-42143
G_A	Gain at Opt Noise Figure	V_{CE} = 10V, I_C = 5 mA	– –	13	– –	dB	MA-42141
		1 GHz		13	– –	dB	MA-42142
		V_{CE} = 10V, I_C = 1.5 mA .45 GHz	– –	18	– –	dB	MA-42143
$\lvert S_{21E}\rvert^2$	Magnitude Forward Transducer Gain, Common Emitter	V_{CE} = 15V, I_C = 15 mA 1 GHz	– –	13	– –	dB	
		2 GHz	6.0	7.5	– –	dB	
		4 GHz	– –	2.0	– –	dB	
G_A (max)	Maximum Available Gain	V_{CE} = 15V, I_C = 15 mA 1 GHz	– –	18.0	– –	dB	
		2 GHz	– –	12.0	– –	dB	

MA-42150 SERIES

specification sheet

npn silicon planar transistors

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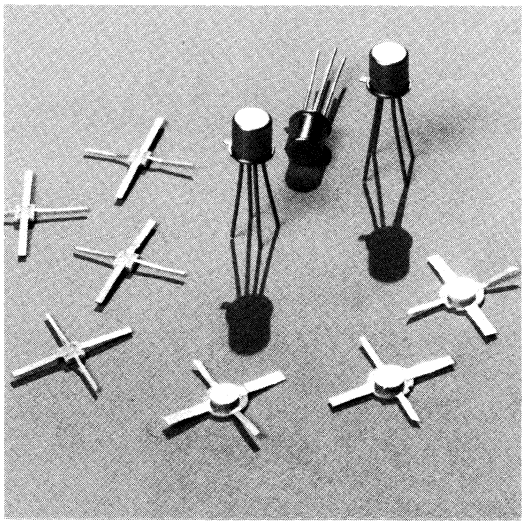
FEATURES

- GUARANTEED POWER OUTPUT @ 3 GHz
- GOLD METALLIZATION
- HIGH RELIABILITY
- RUGGED HERMETIC STRIPLINE PACKAGE
- LOW COST

DESCRIPTION

The MA-42151 npn silicon planar transistor is characterized for oscillator use in the 1.0 – 3.0 GHz frequency range. This transistor when mounted in a common-emitter package exhibits a typical f_{max} of 9.5 GHz at 20 mA collector current.

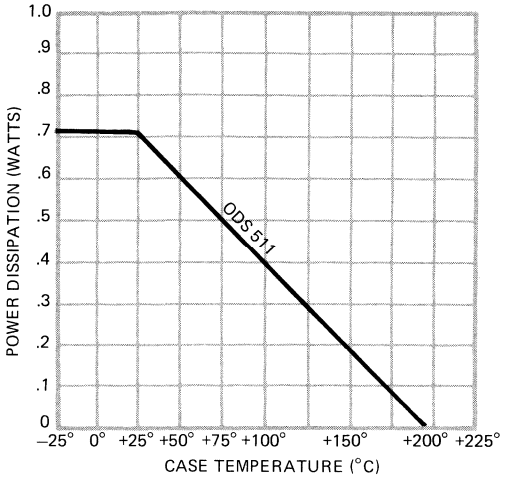
The MA-42151 is available in the hermetically sealed ODS-510 and 511 stripline package and meets the MIL-S-19500 environmental ratings and test requirements of MIL-STD-750/883.



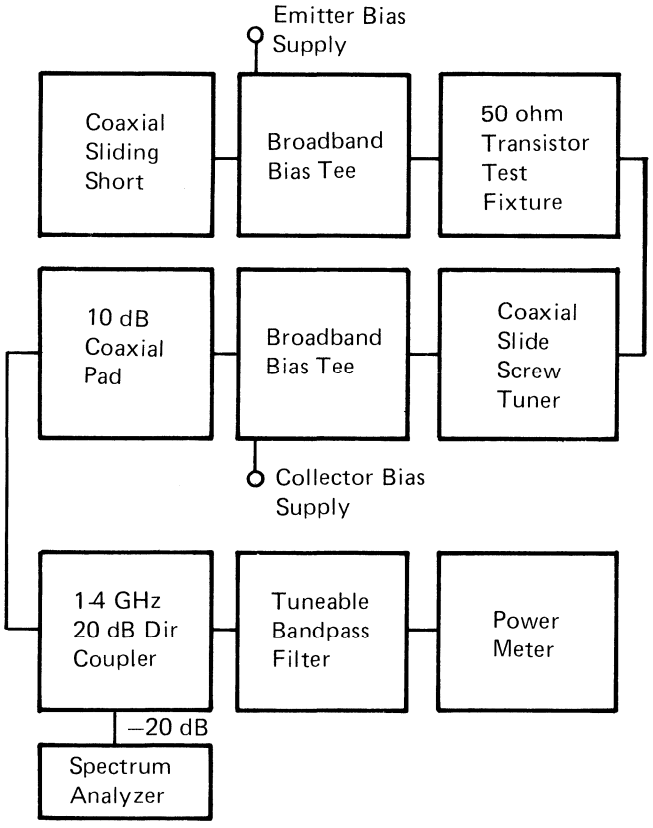
APPLICATIONS

Local oscillators up to 3 GHz

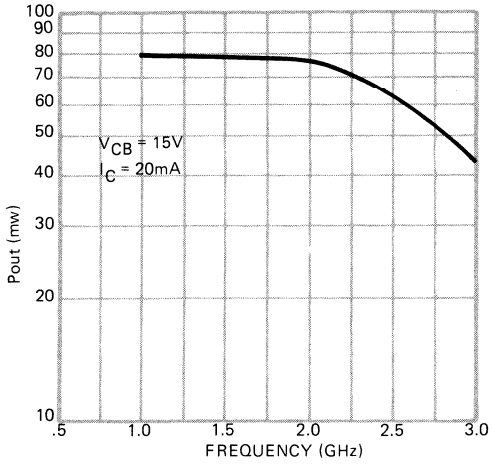
specification sheet



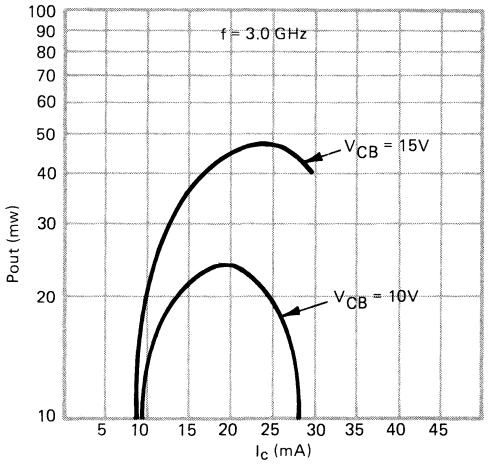
POWER DISSIPATION VS CASE TEMPERATURE



BLOCK DIAGRAM OF MA-42151 OSCILLATOR TEST CIRCUIT

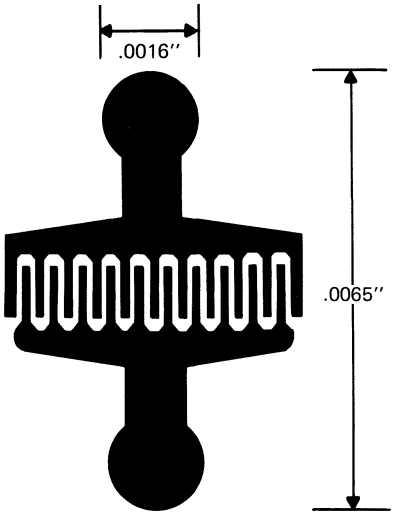


MA-42151-511CB TYPICAL POWER OUTPUT VS FREQUENCY



MA-42151-511CB TYPICAL POWER OUTPUT VS COLLECTOR CURRENT

specification sheet



GEOMETRY 63

ELECTRICAL CHARACTERISTICS (Case temperature 25°C)

Symbol	Definition	Conditions	Min.	Typ.	Max.
BV_{CBO}	Collector-base breakdown voltage	I_C = 10 μA	27V	35V	
BV_{EBO}	Emitter-base breakdown voltage	I_E = 10 μA	3V	3.5V	
BV_{CEO}	Collector-Emitter	I_C = 500 μA	20V	25V	
I_{CBO}	Collector-cut-off current	V_{CB} = 10 V			100 nA
h_{FE}	Current transfer ratio	V_{CE} = 10 V, I_C = 5 mA	20		200
C_{CB}	Output Capacitance	V_{CB} = 15 V			1.0 pF
P_O	Oscillator Power Output	V_{CB} = 10 V, I_C = 20 mA, F = 3 GHz	20mW	25mW	

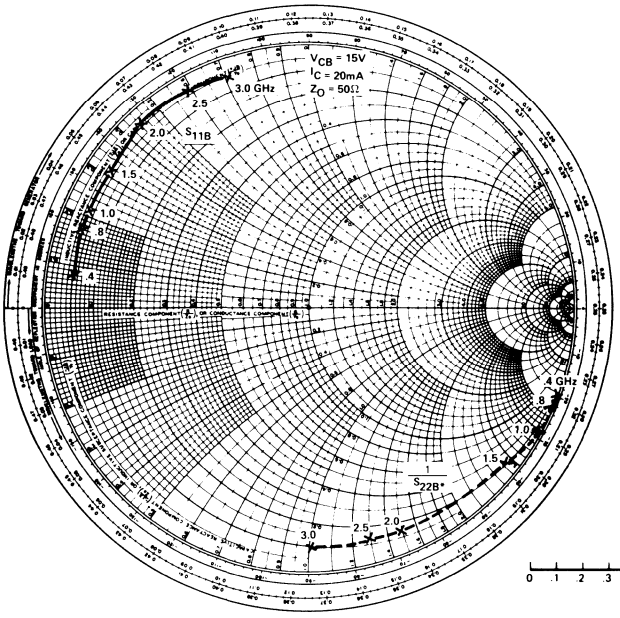
MAXIMUM RATINGS
(Case Temperature 25°C unless otherwise noted)

Total Device Power Dissipation	511 Case - 700 mW
V_{CBO} Collector to Base Voltage	27 V
V_{EBO} Emitter to Base Voltage	3 V
I_C Collector Current	50 mA
Storage Temperature	–65 to +200°C
Operation Junction Temperature	+200°C
Hermeticity	5 x $(10)^{-8}$ cc/sec of He
Lead Temperature (soldering – 10 seconds each lead)	250°C

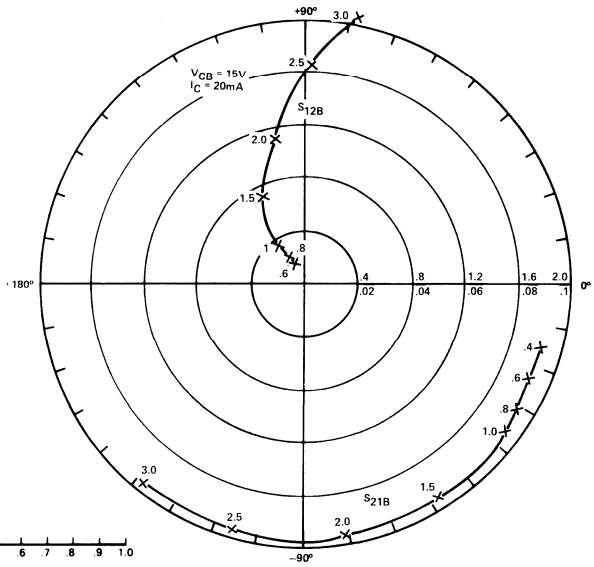
ENVIRONMENTAL RATINGS PER MIL-STD-750

	Method	Level
Storage Temperature	1031	–65 to +200°C
Temperature Cycle	1051	10 cycles –65 to +200°C
Shock	2016	500 g's
Vibration	2056	15 g's
Constant Acceleration	2006	20,000 g's
Humidity	1021	10 days

specification sheet



TYPICAL S_{11B} AND S_{22B} VS FREQUENCY



TYPICAL S_{21B} AND S_{12B} VS FREQUENCY

MA-42151-511 CB
TYPICAL COMMON BASE S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CB} = 15 VOLTS, I_C = 20 mA, Z_G = Z_L = 50 Ω

FREQUENCY (GHz)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
	$\|S_{11B}\|$	ϕS_{11B}	$\|S_{21B}\|$	ϕS_{21B}	$\|S_{12B}\|$	ϕS_{12B}	$\|S_{22B}\|$	ϕS_{22B}
.4	.90	172°	1.89	−14°	.005	103°	.98	−20°
.6	.86	163°	1.88	−23°	.008	110°	1.01	−22°
.8	.90	161°	1.86	−29°	.012	113°	1.01	−26°
1.0	.90	157°	1.90	−35°	.017	115°	.99	−28°
1.2	.90	152°	1.91	−43°	.023	115°	1.03	−31°
1.4	.91	147°	1.93	−52°	.030	113°	1.03	−35°
1.6	.91	142°	1.90	−60°	.037	112°	1.06	−38°
1.8	.91	137°	1.89	−69°	.046	109°	1.08	−43°
2.0	.94	132°	1.95	−79°	.056	99°	1.10	−66°
2.2	.94	128°	1.95	−90°	.066	94°	1.11	−69°
2.4	.93	123°	1.96	99°	.077	90°	1.10	−72°
2.6	.93	118°	1.96	−109°	.087	85°	1.12	−76°
2.8	.93	113°	1.94	−119°	.096	80°	1.14	−83°
3.0	.92	107°	1.89	−130°	.107	78°	1.11	−89°
3.2	.89	103°	1.81	−139°	.122	74°	1.15	−91°
3.4	.87	98°	1.70	−150°	.130	69°	1.15	−95°
3.5	.85	94°	1.65	−160°	.137	61°	1.13	−107°
3.8	.84	90°	1.65	−172°	.149	56°	1.16	−113°
4.0	.80	99°	1.51	−157°	.155	65°	1.25	−113°
4.2	.78	95°	1.43	−170°	.162	58°	1.19	−122°
4.4	.76	93°	1.36	−177°	.167	52°	1.21	−129°
4.6	.74	91°	1.25	170°	.172	48°	1.16	−139°
4.8	.73	89°	1.19	161°	.172	41°	1.11	−144°
5.0	.72	87°	1.10	151°	.176	35°	1.12	−152°
5.2	.73	84°	1.04	143°	.177	30°	1.10	−159°
5.4	.71	79°	.97	135°	.176	23°	1.06	−167°
5.6	.67	77°	.92	127°	.165	19°	1.00	−170°
5.8	.66	74°	.87	118°	.160	15°	.97	−174°
6.0	.65	70°	.83	112°	.156	12°	.96	−178°

specification sheet

npn silicon planar transistors

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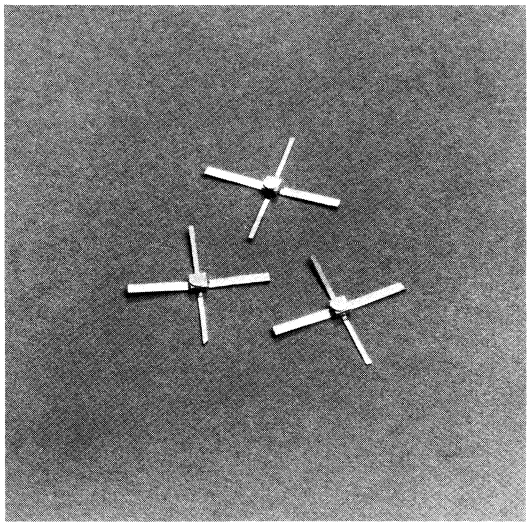
FEATURES

- HIGH POWER GAIN – 14.0 dB TYPICAL AT 2.0 GHz
- LOW INTRINSIC NOISE FIGURE AT 2.0 GHz – 2.3 dB TYPICAL
- GOLD METALLIZATION
- HIGH RELIABILITY
- ION IMPLANTATION TECHNIQUES EMPLOYED FOR EXCELLENT PRODUCT CONSISTENCY

DESCRIPTION

The MA-42161 is a silicon planar epitaxial transistor intended for use in microwave amplifier applications in the .5 to 4 GHz frequency range. The performance of this transistor is comparable to the Fairchild FMT-4005. These units feature outstanding high frequency current gain combined with low rb at small collector currents making them excellent low noise transistors.



APPLICATIONS

RF Amplifiers
Low Level Oscillators

MA-42160 SERIES R.F. SPECIFICATIONS (Case Temperature 25° C)

MODEL NO.	MA-42161	MA-42161	MA-42162	MA-42162	2N6618
CASE STYLE	511	511	511	511	511
Test Frequency (GHz)	1.0	2.0	1.0	2.0	2.0
Max. Noise Fig. @ I_C (dB)	1.5	2.5	1.9	3.0	2.2
G_u (Max) Typ (dB)	18	12	18	12	12
1 dB Compression Point (dBm)	–5	–5	–5	–5	–5
$\lvert S_{21E} \rvert^2$ Typical (dB)	12.5	8.0	12.5	8.0	8.0
Typical Gain (Ga) @ Optimum Noise Figure	15.0	11.0	15.0	11.0	11.0 min
Test Conditions I_C (mA)/V_{CE} (V)	3/10	3/10	3/10	3/10	3/10

specification sheet

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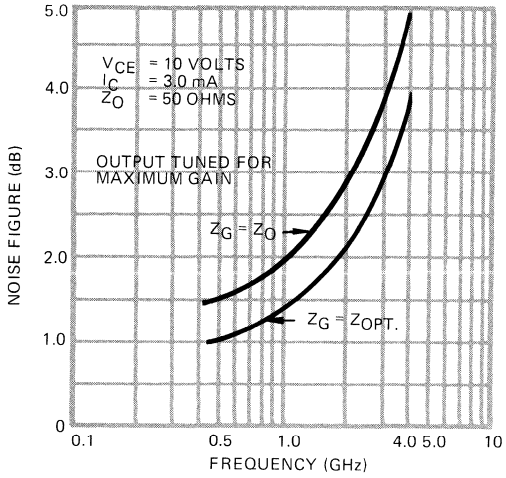
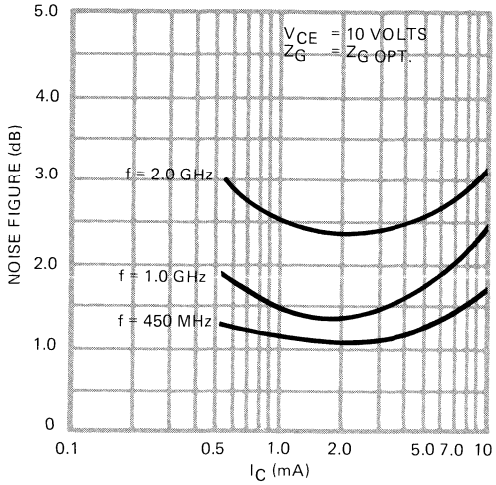
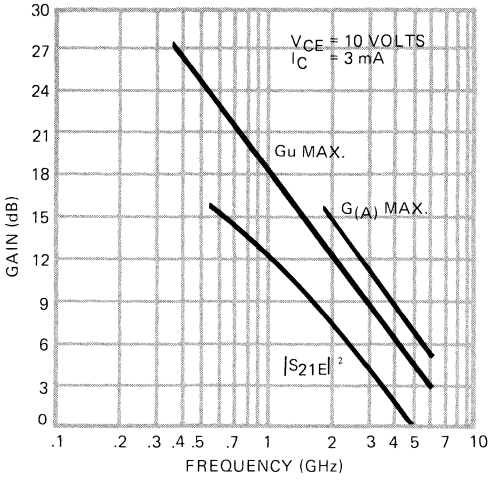


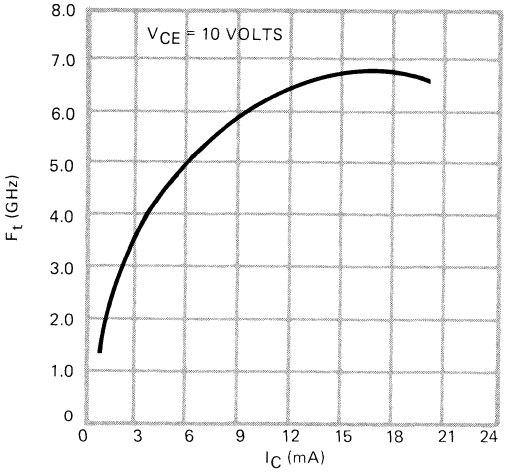
TYPICAL NOISE FIGURE VS FREQUENCY



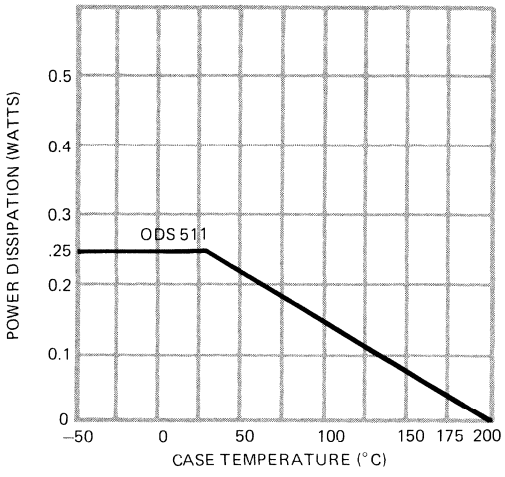
TYPICAL NOISE FIGURE VS COLLECTOR CURRENT



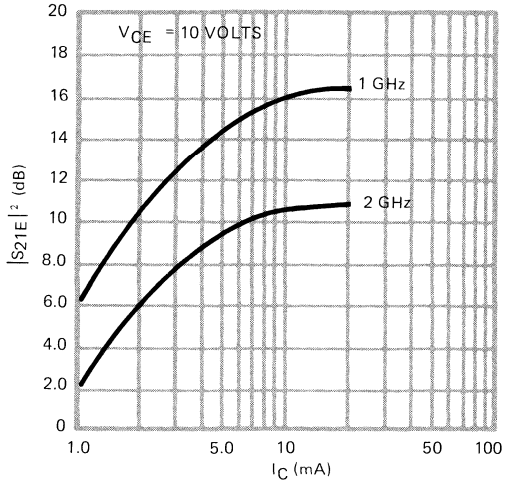
TYPICAL GAIN PARAMETERS VS FREQUENCY



TYPICAL F_T VS COLLECTOR CURRENT

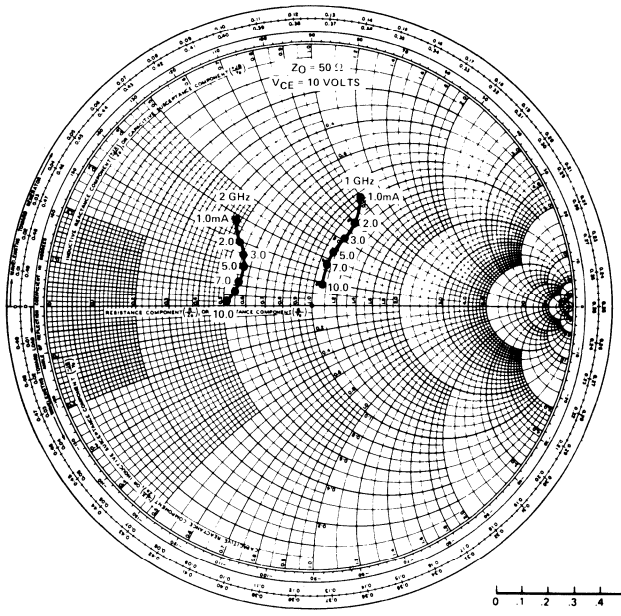


POWER DISSIPATION VS CASE TEMPERATURE

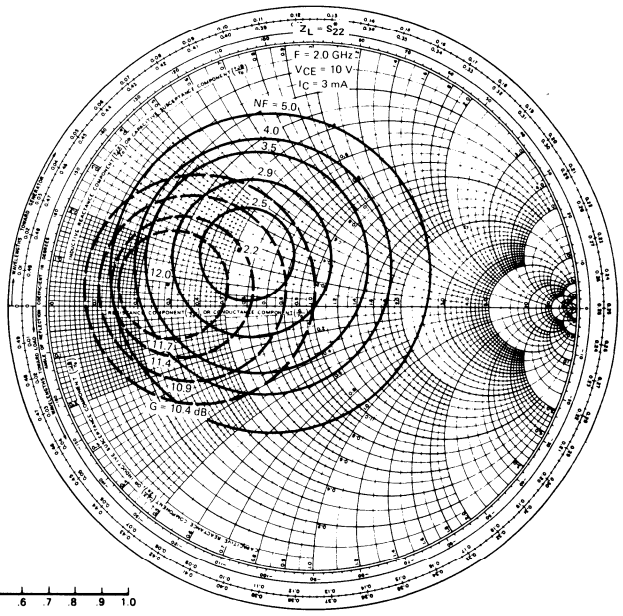


TYPICAL GAIN $|S_{21E}|^2$ VS COLLECTOR CURRENT

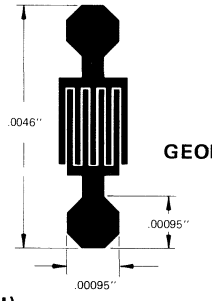
specification sheet



TYPICAL OPTIMUM GENERATOR IMPEDANCE VS COLLECTOR CURRENT



TYPICAL CONSTANT GAIN AND NOISE FIGURES CIRCLES



GEOMETRY 72

MAXIMUM RATING
(Case Temperature 25°C unless otherwise noted)

Maximum Temperatures	
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	200°C
Lead Temperature (60 seconds)	250°C
Total Device Power Dissipation	511 Case −0.25 W
V_{CBO} Collector to Base Voltage	20 V
V_{CEO} Collector to Emitter Voltage	12 V
V_{EBO} Emitter to Base Voltage	1.5 V
I_C Continuous Collector Current	20 mA

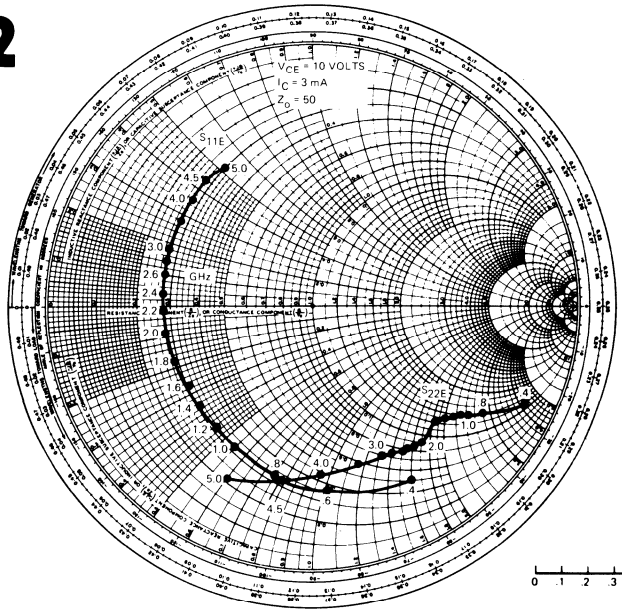
ENVIRONMENTAL RATINGS PER MIL-STD-750

	Method	Level
Storage Temperature	1031	−65 to +200°C
Temperature Cycle	1051	10 cycles −65 to +200°C
Shock	2016	500 g's
Vibration	2056	15 g's
Constant Acceleration	2006	20,000 g's
Humidity	1021	10 days

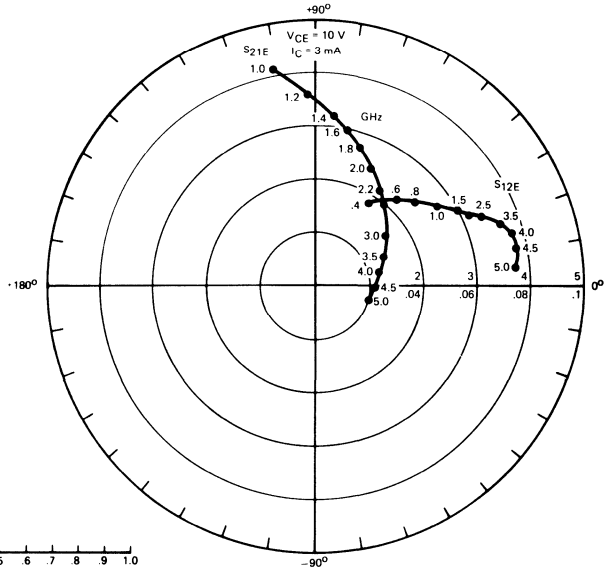
ELECTRICAL CHARACTERISTICS (25°C Ambient Temperature unless otherwise noted)

Symbol	Definition	Conditions	Min.	Typ.	Max.	Units
h_{FE}	DC Current Gain	V_{CE} = 10V, I_C = 3.0 mA	20	80	300	
h_{FE} (2N6618)			50		350	
C_{cb}	Collector to Base Capacitance	V_{CE} = 10V			3.0	pF
BV_{CBO}	Collector to Base Breakdown Voltage	I_C = 10 μA	20	30		V
BV_{CES} (2N6618)	Collector to Base Breakdown Voltage	I_C = 100 μA	30			V
V_{CEO} (sus)	Collector to Emitter Sustaining Voltage	I_C = 1.0 mA	12	17		V
I_{CBO}	Collector Cutoff Current	V_{CB} = 10V			0.01	μA

specification sheet



TYPICAL S_{11E} AND S_{22E} VS FREQUENCY



TYPICAL S_{21E} AND S_{12E} VS FREQUENCY

MA-42161-511
TYPICAL COMMON EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
I_C = 3.0 mA, V_{CE} = 10 VOLTS, $Z_G = Z_L$ = 50 Ω

FREQUENCY (MHz)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
	S_{11E}	ϕS_{11E}	S_{21E}	ϕS_{21E}	S_{12E}	ϕS_{12E}	S_{22E}	ϕS_{22E}
400	.763	– 61.8°	6.826	137.9°	.038	67.8°	.896	– 25.3°
600	.713	– 84.7°	5.748	121.5°	.047	46.4°	.821	– 29.8°
800	.667	–103.0°	4.869	110.4°	.054	39.4°	.765	– 33.1°
1000	.618	–119.9°	4.258	99.2°	.057	33.9°	.719	– 36.0°
1200	.593	–131.7°	3.744	91.7°	.060	30.5°	.705	– 35.4°
1400	.578	–143.9°	3.293	83.7°	.062	28.9°	.695	– 38.5°
1600	.559	–154.9°	2.989	76.8°	.063	25.9°	.681	– 40.6°
1800	.565	–163.4°	2.769	68.8°	.064	23.5°	.650	– 43.0°
2000	.557	–171.0°	2.453	63.5°	.065	24.1°	.667	– 51.9°
2200	.557	–179.0°	2.241	56.0°	.066	21.6°	.653	– 54.1°
2400	.557	174.2°	2.078	51.2°	.068	20.1°	.651	– 56.0°
2600	.550	167.7°	1.939	46.8°	.066	20.0°	.638	– 59.5°
2800	.565	162.2°	1.854	40.0°	.069	20.1°	.626	– 61.8°
3000	.582	156.9°	1.720	35.9°	.069	20.5°	.618	– 55.1°
3200	.577	152.3°	1.815	29.9°	.071	19.1°	.644	– 69.1°
3400	.586	147.0°	1.551	26.1°	.073	19.3°	.639	– 74.8°
3600	.593	142.9°	1.434	20.4°	.072	17.1°	.630	– 78.4°
3800	.699	138.5°	1.387	15.2°	.074	15.7°	.626	– 83.3°
4000	.612	136.2°	1.275	12.2°	.077	15.8°	.654	– 88.1°
4200	.610	132.3°	1.220	5.2°	.076	13.2°	.653	– 93.6°
4400	.612	130.0°	1.159	1.7°	.078	13.2°	.659	– 97.5°
4600	.616	125.6°	1.089	–4.3°	.076	10.1°	.683	–104.4°

MA-42180 SERIES

specification sheet

npn silicon planar transistors

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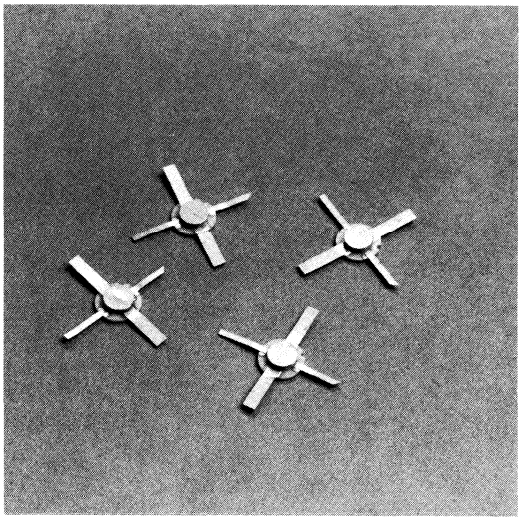
FEATURES

- HIGH POWER GAIN AT 1 GHz (14.5 dB)
- GOLD METALLIZATION
- HIGH RELIABILITY
- EXCELLENT WIDE DYNAMIC RANGE (+37 dBm 3RD ORDER INTERCEPT)

DESCRIPTION

The MA-42181 npn silicon planar transistor is designed for wide dynamic range amplifier applications over the .1 to 3 GHz frequency range. This transistor exhibits a 14.5 dB gain at 1 GHz when tuned as an amplifier in a maximum gain condition. While under these same conditions, the 1 dB compression point is +25 dBm and the 3rd order intercept point has been measured at +37 dBm. The MA-42181 is supplied in the common-emitter configuration.

The MA-42181 is available in the hermetically sealed ODS-510 stripline package and meets the MIL-S-19500 environmental ratings and test requirements of MIL-STD-750/883.



APPLICATIONS

RF Amplifiers
Low Level Oscillators
Second Stage Amplifiers

HIGH FREQUENCY CHARACTERISTICS

Symbol	Conditions	Min.	Typ.	Units
$\|S_{21E}\|^2$	V_{CE} = 15V, I_C = 60 mA, F = 1 GHz	6.0	8.0	dB
	F = 2 GHz	— —	2.0	dB
G_U(max)	V_{CE} = 15V, I_C = 60 mA, F = 1 GHz		13.0	dB
	F = 2 GHz		8.4	dB
GA (max)	V_{CE} = 15V, I_C = 60 mA, F = 1 GHz		14.5	dB
f_{max}	V_{CE} = 15V, I_C = 60 mA		6.5	GHz
Compression Point (1-dB)	V_{CE} = 15V, I_C = 60 mA, $Z_G = Z_L$ = 50 Ω F = 1 GHz			
	Untuned		+20	dBm
	Tuned		+25	dBm
3rd Order Intercept	V_{CE} = 15V, I_C = 60 mA, $Z_G = Z_L$ = 50Ω F = 1 GHz			
	Untuned		+33	dBm
	Tuned		+37	dBm

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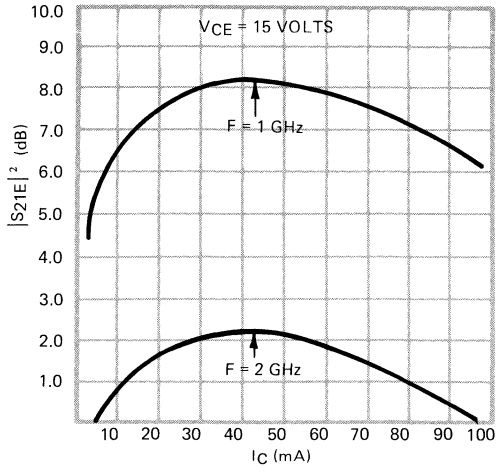
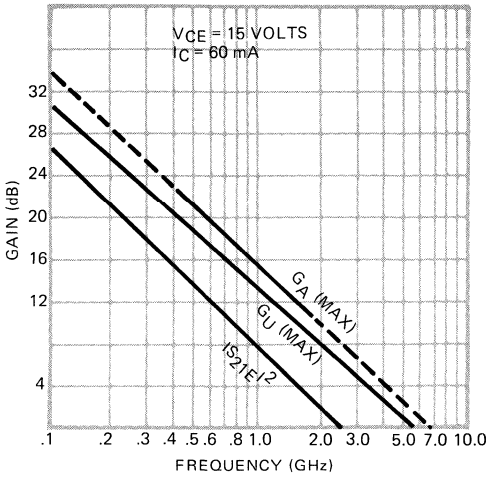


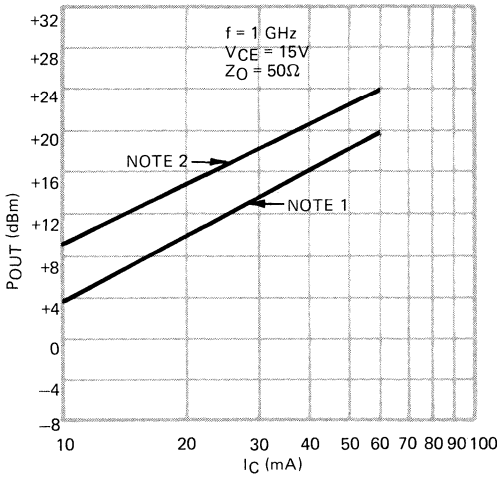
TYPICAL $|S_{21E}|^2$ VS COLLECTOR CURRENT



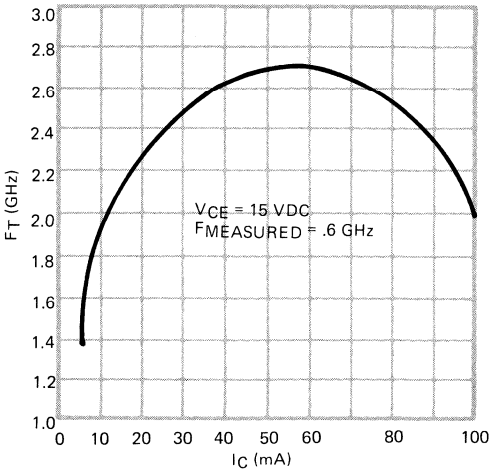
TYPICAL GAIN PARAMETERS VS FREQUENCY

NOTE 1. $Z_G = Z_L = Z_O$

NOTE 2. TRANSISTOR INPUT AND OUTPUT TUNED FOR MAXIMUM AVAILABLE GAIN



TYPICAL P_{OUT} @ 1 dB COMPRESSION VS COLLECTOR CURRENT



TYPICAL F_T VS COLLECTOR CURRENT

specification sheet

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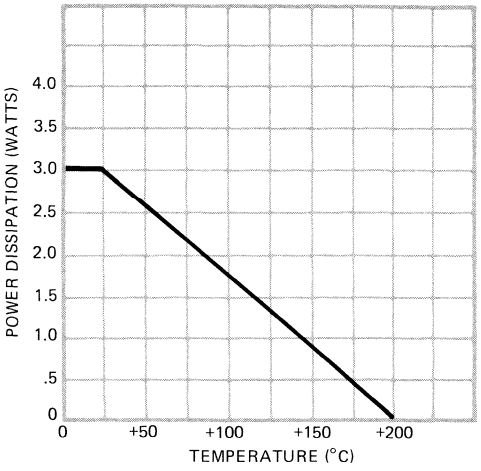
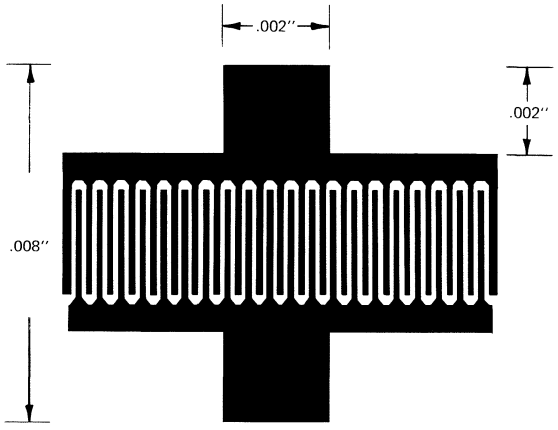


POWER DISSIPATION VS CASE TEMPERATURE



GEOMETRY 02

ELECTRICAL CHARACTERISTICS

Symbol	Conditions	Min.	Typ.	Max.	Units
BV_{CEO}	I_C = 100 μA	25	29	— —	V
BV_{CBO}	I_C = 100 μA	30	40	— —	V
BV_{EBO}	I_E = 10 μA	3.5	5.0	— —	V
h_{FE}	V_{CE} = 5V, I_C = 100 mA	25	— —	— —	

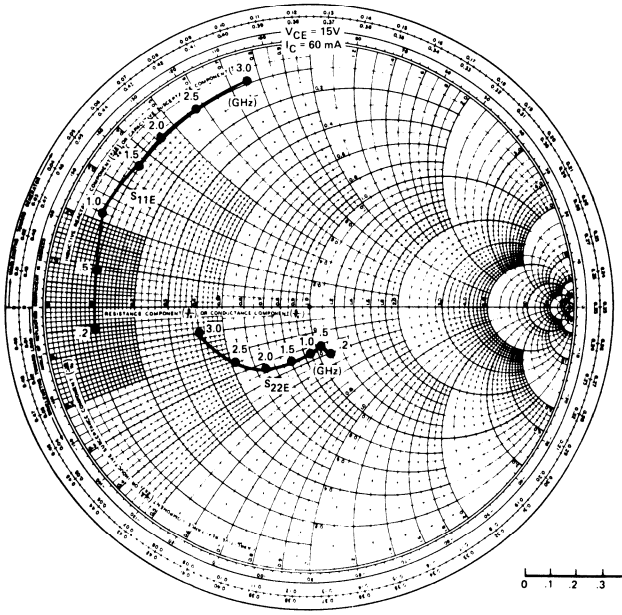
MAXIMUM RATING
(Case Temperature 25°C unless otherwise noted)

Total Device Power	510 Case — 3.0 W
V_{CBO} Collector to Base Voltage	30 V
V_{EBO} Emitter to Base Voltage	3.5 V
V_{CEO} Collector to Emitter Voltage	25 V
Collector Current	300 mA
Storage Temperature	–65 to +200°C
Hermeticity	5 x $(10)^{-8}$ cc/sec of He
Operation Junction Temperature	+200°C
Lead Temperature (Soldering — 10 Seconds each lead)	230°C

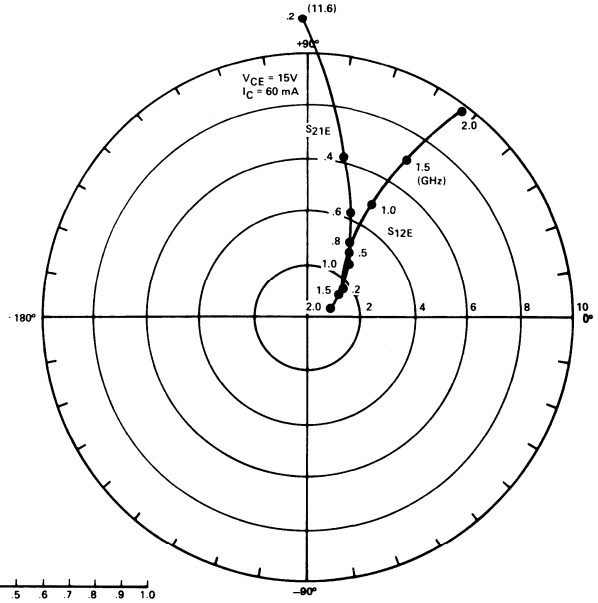
ENVIRONMENTAL RATINGS PER MIL-STD-750

	Method	Level
Storage Temperature	1031	–65 to +200°C
Temperature Cycle	1051	10 cycles –65 to +200°C
Shock	2016	500 g's
Vibration	2056	15 g's
Constant Acceleration	2006	20,000 g's
Humidity	1021	10 days

specification sheet



TYPICAL S_{11E} AND S_{22E} VS FREQUENCY



TYPICAL S_{12E} AND S_{21E} VS FREQUENCY

MA-42181-510
TYPICAL COMMON EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 15 VOLTS, I_C = 60 mA

FREQUENCY (MHz)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
	$\|S_{11E}\|$	ϕS_{11E}	$\|S_{21E}\|$	ϕS_{21E}	$\|S_{12E}\|$	ϕS_{12E}	$\|S_{22E}\|$	ϕS_{22E}
200.0	.808	−175.8°	11.586	87.9°	.017	30.9°	.189	−63.0°
400.0	.817	173.8°	6.045	76.7°	.022	44.3°	.153	−64.9°
600.0	.818	166.9°	4.132	66.1°	.031	54.5°	.150	−71.8°
800.0	.822	159.6°	3.153	57.4°	.039	55.6°	.162	−78.8°
1000.0	.825	153.7°	2.546	49.8°	.047	57.4°	.171	−86.4°
1200.0	.848	148.6°	2.164	42.3°	.056	57.3°	.190	−96.4°
1400.0	.833	144.1°	1.858	34.5°	.065	56.4°	.213	−101.9°
1600.0	.836	137.7°	1.628	27.1°	.075	55.3°	.225	−111.2°
1800.0	.847	132.0°	1.438	20.0°	.083	51.5°	.257	−121.0°
2000.0	.864	131.3°	1.275	14.5°	.099	52.1°	.282	−125.9°
2200.0	.857	126.2°	1.164	6.0°	.114	48.7°	.306	−135.0°
2400.0	.871	119.7°	1.076	.3°	.135	43.9°	.327	−142.1°
2600.0	.873	117.1°	.980	−5.4°	.134	32.1°	.368	−149.6°
2800.0	.897	111.4°	.879	−12.4°	.147	36.8°	.382	−157.4°
3000.0	.860	104.7°	.804	−19.6°	.186	32.4°	.420	−166.5°

MA-42181-510
TYPICAL COMMON EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 15 VOLTS, I_C = 15 mA

FREQUENCY (MHz)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
	$\|S_{11E}\|$	ϕS_{11E}	$\|S_{21E}\|$	ϕS_{21E}	$\|S_{12E}\|$	ϕS_{12E}	$\|S_{22E}\|$	ϕS_{22E}
200.0	.803	−164.5°	10.758	92.3°	.027	28.3°	.303	−55.1°
400.0	.811	179.4°	5.674	79.0°	.031	29.9°	.233	−57.3°
600.0	.825	170.6°	3.869	67.5°	.034	35.9°	.224	−63.9°
800.0	.816	162.5°	2.930	58.4°	.039	39.9°	.232	−71.2°
1000.0	.822	155.9°	2.375	50.5°	.045	46.1°	.238	−79.2°
1200.0	.849	150.3°	2.024	43.0°	.052	47.9°	.259	−89.4°
1400.0	.832	145.6°	1.739	34.8°	.060	49.4°	.278	−96.9°
1600.0	.836	139.0°	1.524	27.5°	.071	50.4°	.289	−106.3°
1800.0	.846	133.2°	1.345	20.5°	.080	49.5°	.315	−116.4°
2000.0	.864	132.3°	1.192	15.1°	.092	50.0°	.346	−122.6°
2200.0	.856	127.0°	1.085	7.3°	.108	47.1°	.366	−132.3°
2400.0	.870	120.4°	1.000	1.0°	.129	43.5°	.382	−139.6°
2600.0	.868	117.6°	.916	−4.0°	.133	31.1°	.422	−147.8°
2800.0	.894	111.9°	.818	−11.3°	.144	35.6°	.434	−155.9°
3000.0	.858	105.2°	.749	−18.2°	.182	31.9°	.464	−164.8°

MA-42190 SERIES

specification sheet

npn silicon planar transistors

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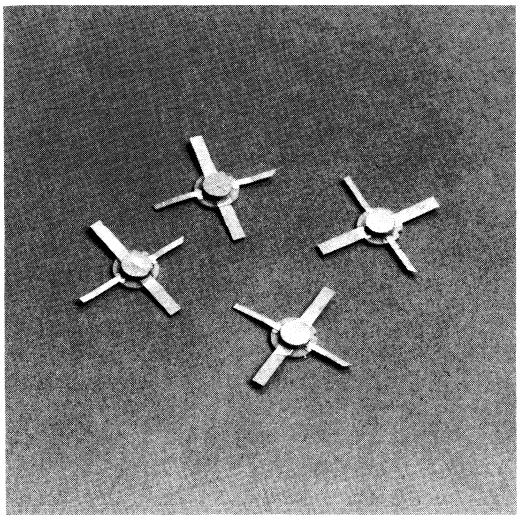
FEATURES

- GUARANTEED POWER OUTPUT @ 2.0 GHz
- GOLD METALLIZATION
- HIGH RELIABILITY
- RUGGED HERMETIC STRIPLINE PACKAGE

DESCRIPTION

The MA-42191 npn silicon planar transistor is characterized for oscillator use in the 1.0 – 3.0 GHz frequency range. This transistor when mounted in a common-emitter package exhibits a typical f_{max} of 6.0 GHz at 50 mA collector current.

The MA-42191 is available in the hermetically sealed ODS-510 stripline package and meets the MIL-S-19500 environmental ratings and test requirements of MIL-STD-750/883.



APPLICATIONS

Moderate Power Oscillators up to 3 GHz

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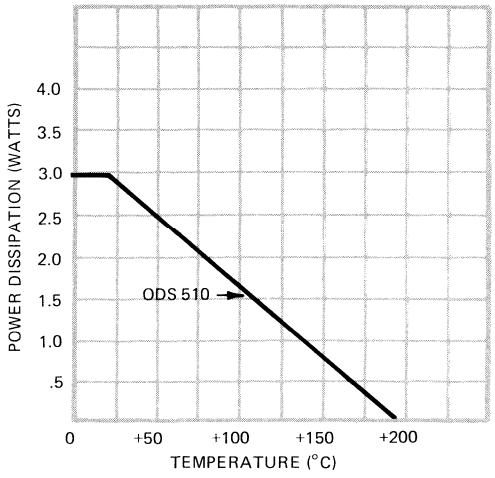
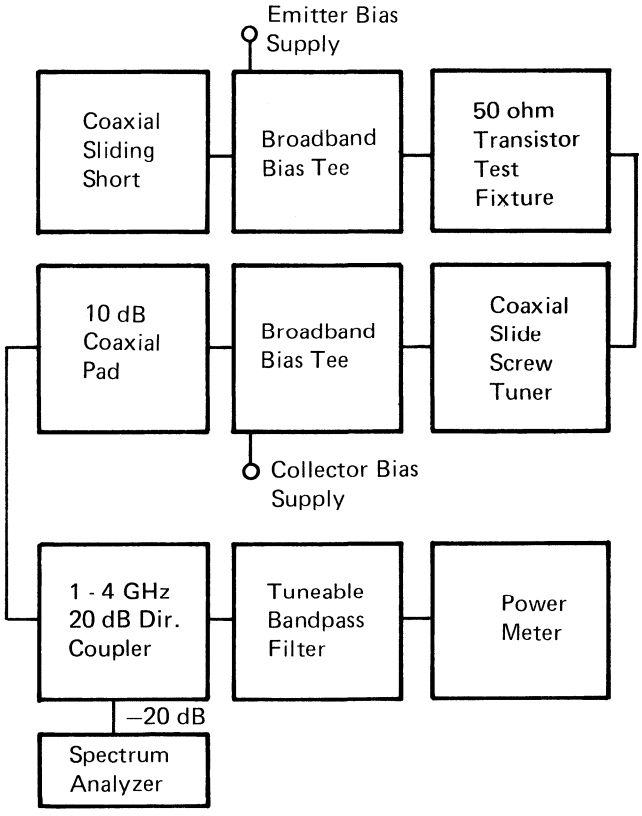
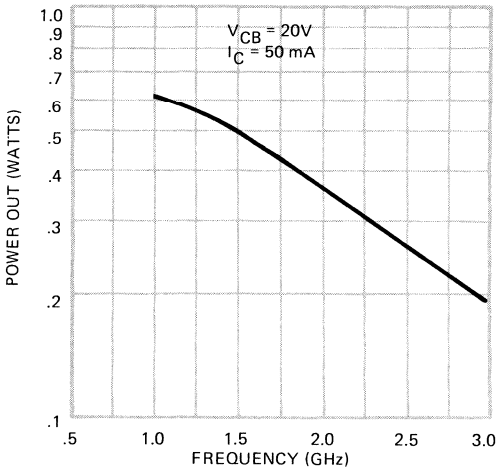


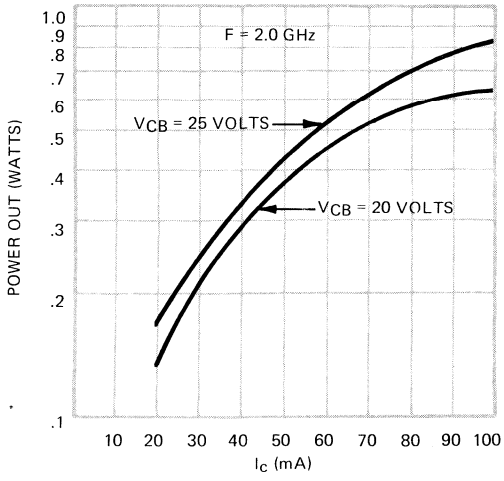
POWER DISSIPATION VS CASE TEMPERATURE



MA-42191 BLOCK DIAGRAM OF OSCILLATOR TEST CIRCUIT

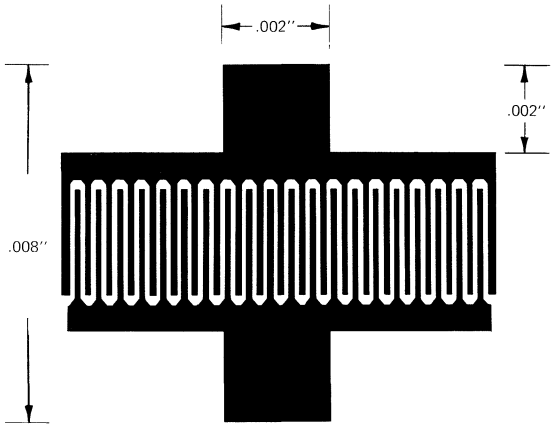


TYPICAL P_{OUT} VS FREQUENCY



TYPICAL P_{OUT} VS COLLECTOR CURRENT

specification sheet



GEOMETRY 02

HIGH FREQUENCY & ELECTRICAL CHARACTERISTICS

Symbol	Definitions	Conditions	Min.	Typ.	Max.	Units
BV_{CEO}	Collector Emitter Breakdown Voltage	I_C = 100 μA	25	29	– –	V
BV_{CBO}	Collector Base Breakdown Voltage	I_C = 100 μA	30	40	– –	V
BV_{EBO}	Emitter Base Breakdown Voltage	I_E = 10 μA	3.5	5.0	– –	V
h_{FE}	Current Transfer Ratio	V_{CE} = 5V, I_C = 100 mA	25	– –	– –	
Po	Oscillator Power Output	V_{CB} = 20V, I_C = 50 mA, F = 2 GHz	350	390	– –	mW
P_o	Oscillator Power Output	V_{CB} = 20V, I_C = 50 mA, F = 1 GHz	– –	650	– –	mW

MAXIMUM RATING
(Case Temperature 25°C unless otherwise noted)

Total Device Power	510 Case – 3.0 W
VCBO Collector to Base Voltage	30 V
V_{EBO} Emitter to Base Voltage	3.5 V
V_{CEO} Collector to Emitter Voltage	25 V
Collector Current	300 mA
Storage Temperature	–65 to +200°C
Hermeticity	5 x $(10)^{-8}$ cc/sec of He
Operating Junction Temperature	+200°C
Lead Temperature (Soldering – 10 Seconds each lead)	230°C

ENVIRONMENTAL RATINGS PER MIL-STD-750

	Method	Level
Storage Temperature	1031	–65 to +200°C
Temperature Cycle	1051	10 cycles –65 to +200°C
Shock	2016	500 g's
Vibration	2056	15 g's
Constant Acceleration	2006	20,000 g's
Humidity	1021	10 days

specification sheet

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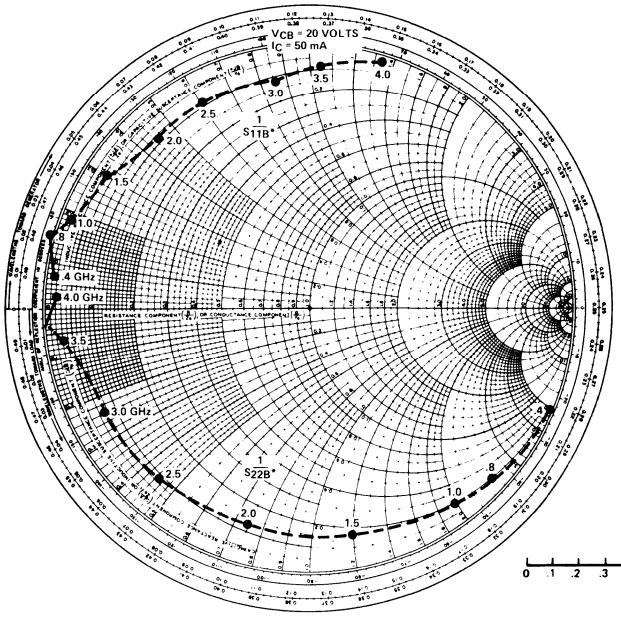
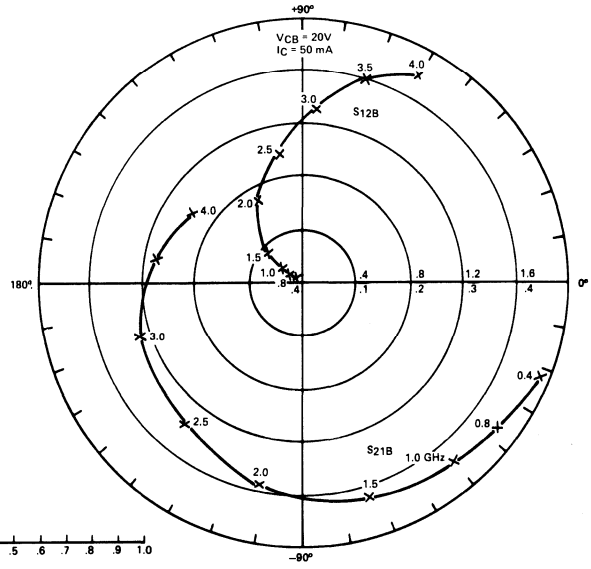


TYPICAL S_{11B} AND S_{22B} VS FREQUENCY



TYPICAL S_{21B} AND S_{12B} VS FREQUENCY

MA-42191-510
TYPICAL COMMON BASE S-PARAMETERS AT 25°C LEAD TEMPERATURE
I_C = 50 mA, V_{CB} = 20 VOLTS, Z_G = Z_L = 50 Ω

FREQUENCY (GHz)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
	$\|S_{11B}\|$	ϕS_{11B}	$\|S_{21B}\|$	ϕS_{21B}	$\|S_{12B}\|$	ϕS_{12B}	$\|S_{22B}\|$	ϕS_{22B}
.40	.973	172.3°	1.933	−20.7°	.007	133.6°	1.014	−23.3°
.60	.968	168.7°	1.894	−30.2°	.015	142.3°	1.033	−33.4°
.80	1.006	164.2°	1.854	−39.8°	.026	143.8°	1.060	−43.6°
1.00	1.038	160.0°	1.797	−50.2°	.039	141.8°	1.070	−53.9°
1.20	1.042	155.7°	1.734	−59.1°	.055	139.7°	1.086	−63.4°
1.40	1.063	150.8°	1.717	−70.0°	.073	137.7°	1.111	−74.0°
1.60	1.077	145.1°	1.621	−78.7°	.103	133.1°	1.144	−84.5°
1.80	1.109	138.8°	1.567	−88.1°	.136	127.3°	1.176	−93.5°
2.00	1.155	131.6°	1.517	−102.2°	.170	120.7°	1.164	−105.6°
2.20	1.168	126.6°	1.409	−111.5°	.212	113.1°	1.148	−116.0°
2.40	1.150	121.0°	1.374	−124.1°	.231	107.6°	1.163	−126.2°
2.60	1.119	114.1°	1.303	−136.0°	.274	100.7°	1.168	−135.6°
2.80	1.123	106.3°	1.335	−149.0°	.318	92.8°	1.168	−143.9°
3.00	1.132	99.2°	1.239	−160.8°	.339	86.6°	1.120	−152.6°
3.20	1.143	93.5°	1.238	−173.0°	.370	79.6°	1.094	−160.2°
3.40	1.106	89.5°	1.129	176.8°	.394	77.4°	1.069	−167.9°
3.60	1.053	83.1°	1.085	161.6°	.401	70.2°	1.021	−175.5°
3.80	1.024	75.1°	1.110	151.0°	.458	63.5°	.976	178.0°
4.00	1.019	74.1°	1.097	148.9°	.450	60.8°	.960	176.9°

MA-42191-510
TYPICAL COMMON BASE S-PARAMETERS AT 25°C LEAD TEMPERATURE
I_C = 30.0 mA, V_{CB} = 20.0 VOLTS, Z_G = Z_L = 50 Ω

FREQUENCY (GHz)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
	$\|S_{11B}\|$	ϕS_{11B}	$\|S_{21B}\|$	ϕS_{21B}	$\|S_{12B}\|$	ϕS_{12B}	$\|S_{22B}\|$	ϕS_{22B}
.40	.966	172.5°	1.916	−20.7°	.007	132.9°	1.013	−23.1°
.60	.970	168.6°	1.876	−30.7°	.015	140.6°	1.033	−33.3°
.80	.991	164.3°	1.833	−40.5°	.026	142.4°	1.060	−43.5°
1.00	.999	160.0°	1.769	−50.4°	.038	141.0°	1.115	−53.7°
1.20	1.027	155.7°	1.700	−60.0°	.055	138.9°	1.087	−63.6°
1.40	1.047	150.8°	1.679	−70.9°	.072	136.7°	1.108	−74.2°
1.60	1.064	145.2°	1.569	−79.6°	.101	132.5°	1.146	−84.5°
1.80	1.093	138.9°	1.543	−89.3°	.135	126.8°	1.168	−93.2°
2.00	1.137	131.9°	1.465	−103.3°	.167	120.5°	1.159	−105.5°
2.20	1.148	126.9°	1.357	−112.5°	.208	113.0°	1.144	−115.7°
2.40	1.129	121.3°	1.314	−124.7°	.227	107.7°	1.153	−125.6°
2.60	1.099	114.5°	1.236	−136.4°	.268	101.0°	1.150	−134.9°
2.80	1.108	106.8°	1.274	−149.5°	.312	93.2°	1.160	−143.1°
3.00	1.114	99.8°	1.181	−160.9°	.333	87.1°	1.114	−151.6°
3.20	1.128	94.3°	1.185	−172.9°	.365	80.3°	1.089	−159.1°
3.40	1.096	90.2°	1.070	176.6°	.386	78.1°	1.059	−166.9°
3.60	1.039	83.9°	1.041	161.9°	.398	71.2°	1.021	−174.3°
3.80	1.002	75.9°	1.060	151.3°	.452	64.5°	.976	179.1°
4.00	1.005	74.8°	1.058	149.2°	.448	61.6°	.968	178.0°

MA-42191-510
TYPICAL COMMON BASE S-PARAMETERS AT 25°C LEAD TEMPERATURE
I_C = 70.0 mA, V_{CB} = 20.0 VOLTS, $Z_G = Z_L = 50\ \Omega$

FREQUENCY (GHz)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
	$\|S_{11B}\|$	ϕS_{11B}	$\|S_{21B}\|$	ϕS_{21B}	$\|S_{12B}\|$	ϕS_{12B}	$\|S_{22B}\|$	ϕS_{22B}
.40	.976	172.3°	1.929	−21.0°	.007	136.3°	1.016	−23.4°
.50	.986	168.0°	1.894	−31.6°	.016	142.2°	1.034	−33.9°
.80	1.004	164.0°	1.849	−41.3°	.026	142.9°	1.061	−44.1°
1.00	1.015	159.7°	1.790	−51.5°	.039	141.1°	1.081	−54.4°
1.20	1.047	154.9°	1.731	−61.4°	.056	138.9°	1.082	−64.7°
1.40	1.058	150.1°	1.697	−73.0°	.074	136.4°	1.123	−75.6°
1.60	1.076	143.4°	1.588	−82.1°	.105	131.5°	1.146	−85.9°
1.80	1.101	137.7°	1.536	−91.4°	.138	125.6°	1.164	−94.9°
2.00	1.147	130.8°	1.471	−106.5°	.172	118.9°	1.160	−107.3°
2.20	1.155	125.8°	1.360	−116.1°	.212	111.4°	1.127	−117.7°
2.40	1.134	120.3°	1.312	−128.7°	.231	105.7°	1.139	−127.9°
2.60	1.102	113.4°	1.238	−141.3°	.273	99.0°	1.140	−137.2°
2.80	1.103	105.6°	1.260	−154.7°	.314	91.2°	1.133	−145.3°
3.00	1.108	98.6°	1.162	−166.3°	.334	85.2°	1.080	−153.7°
3.20	1.117	93.2°	1.169	−178.4°	.364	78.5°	1.064	−161.0°
3.40	1.062	89.2°	1.055	171.4°	.366	76.5°	1.027	−168.4°
3.60	1.025	83.0°	1.012	156.7°	.393	69.6°	.978	−175.6°
3.80	.996	75.1°	1.036	146.2°	.448	63.2°	.937	178.2°
4.00	.991	74.1°	1.026	144.5°	.442	60.6°	.927	177.5°

MA-42191-510
TYPICAL COMMON BASE S-PARAMETERS AT 25°C LEAD TEMPERATURE
I_C = 100.0 mA, V_{CB} = 20.0 VOLTS, $Z_G = Z_L = 50\ \Omega$

FREQUENCY (GHz)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
	$\|S_{11B}\|$	ϕS_{11B}	$\|S_{21B}\|$	ϕS_{21B}	$\|S_{12B}\|$	ϕS_{12B}	$\|S_{22B}\|$	ϕS_{22B}
.40	.955	171.5°	1.747	−27.5°	.008	104.4°	.986	−26.1°
.60	.967	167.0°	1.671	−39.9°	.016	121.3°	1.005	−37.5°
.80	.980	152.5°	1.583	−51.3°	.028	127.1°	1.024	−49.0°
1.00	.982	158.1°	1.487	−62.5°	.041	126.8°	1.022	−60.6°
1.20	1.009	153.5°	1.385	−74.4°	.058	126.0°	1.019	−70.8°
1.40	1.014	148.1°	1.298	−87.2°	.076	124.0°	1.029	−82.3°
1.60	1.012	142.4°	1.175	−97.2°	.105	120.2°	1.048	−92.9°
1.80	1.029	136.4°	1.095	−107.9°	.133	114.5°	1.039	−102.1°
2.00	1.057	129.4°	.994	−123.1°	.163	108.5°	1.004	−113.7°
2.20	1.058	124.9°	.889	−133.4°	.198	102.5°	.971	−123.3°
2.40	1.033	120.1°	.828	−146.2°	.212	98.0°	.967	−132.3°
2.60	.999	114.0°	.771	−158.7°	.247	92.5°	.962	−140.1°
2.80	.993	106.4°	.768	−171.8°	.283	85.8°	.953	−146.9°
3.00	.999	100.1°	.712	176.9°	.300	81.5°	.910	−154.0°
3.20	1.989	95.3°	.708	165.2°	.328	76.0°	.887	−160.2°
3.40	.979	91.9°	.660	155.3°	.349	74.7°	.862	−166.5°
3.60	.936	86.4°	.650	141.6°	.360	58.7°	.857	−172.6°
3.80	.904	79.0°	.680	132.0°	.411	53.6°	.829	−177.5°
4.00	.902	78.1°	.678	130.2°	.407	60.9°	.824	−178.5°

notes

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2N2857 JAN

specification sheet

npn silicon planar transistors

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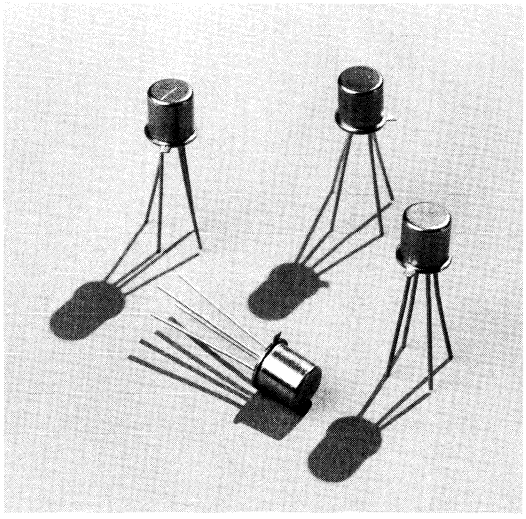
FEATURES

- LOW COST
- GOLD METALLIZATION
- LOW NOISE FIGURE AT LOW I_C
- HIGH GAIN (19 dB G_{PE} @ 450 MHz)
- EXCELLENT RELIABILITY
- USEFUL TO 700 MHz
- 100% TESTED TO JAN SPECIFICATIONS

DESCRIPTION

Designed especially for low cost, high reliability type applications, this series of npn Silicon Planar Transistors offers low noise, high gain performance, which meet or exceed all JAN specifications. These devices are fully tested and screened in accordance with JAN procedures. A 1.8 GHz current gain-bandwidth product (f_T) is typical for this device. The transistors are rugged and employ gold metallization for an unprecedented reliability.



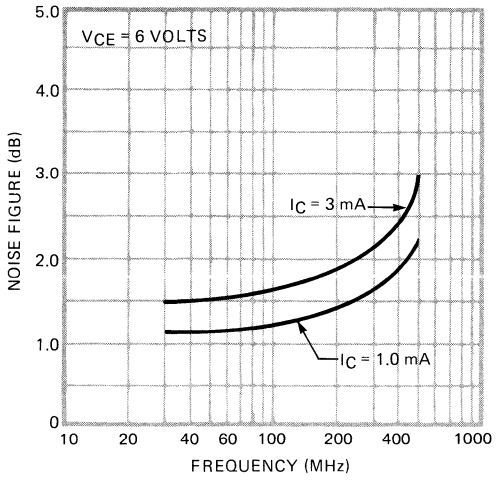
APPLICATIONS

IF, VHF, UHF, TV and RF Amplifiers

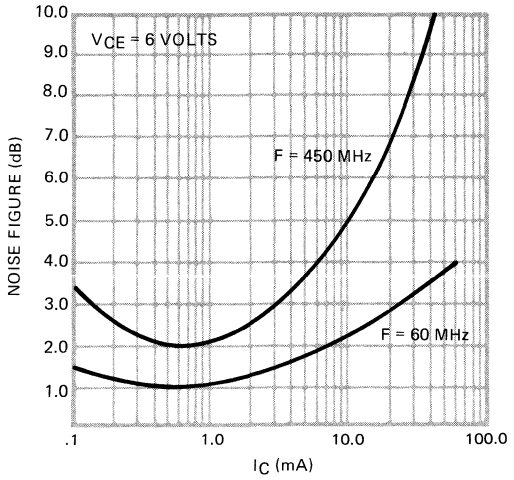
2N2857 JAN HIGH FREQUENCY CHARACTERISTICS (T_A = 25°C Unless Otherwise Specified)

Symbol	Definitions	Conditions	Min.	Typ.	Max.	Unit
N.F.	Noise Figure	V_{CE} = 6V, I_C = 1.5 mA, f = 450 MHz, R_G = 50 ohms, Figure 1	– – –	2.3	4.5	dB
$\lvert h_{fe} \rvert$	Magnitude of C.E. small signal short-circuit transfer ratio	V_{CE} = 6V, I_C = 5 mA, f = 100 MHz	10	14	19	– – –
h_{fe}	Small signal short-circuit forward-current transfer ratio	V_{CE} = 6V, I_C = 2 mA,	50	95	220	– – –
C_{CB}	Collector to base feedback capacitance	V_{CB} = 10V, I_E = 0, f = 1.0 MHz	– – –	.6	1.0	pf
G_{PE}	Small signal power gain	V_{CE} = 6V, I_C = 1.5 mA, f = 450 MHz	12.5	19	21	dB
$r_b' C_C$	Collector base time constant	V_{CB} = 6V, I_E = 2 mA, f = 31.9 MHz, Figure 2	4	7	15	psec
Po**	Oscillator Power output	Oscillator power output f = 500 MHz, V_{CB} = 10 V, I_E = 12 mA	30	55	– – –	mW

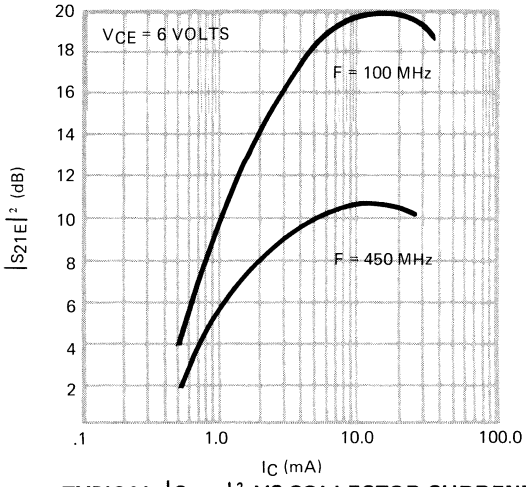
specification sheet



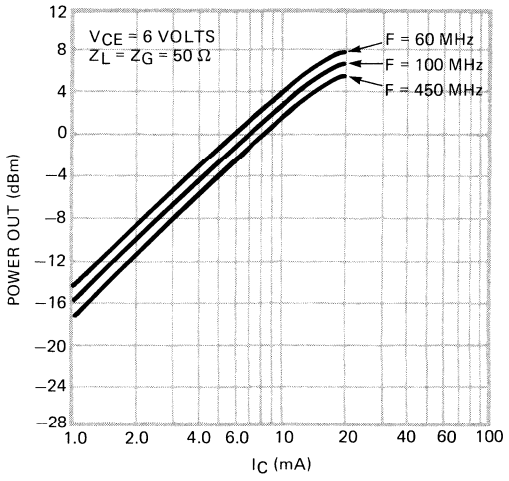
TYPICAL NOISE FIGURE VS FREQUENCY



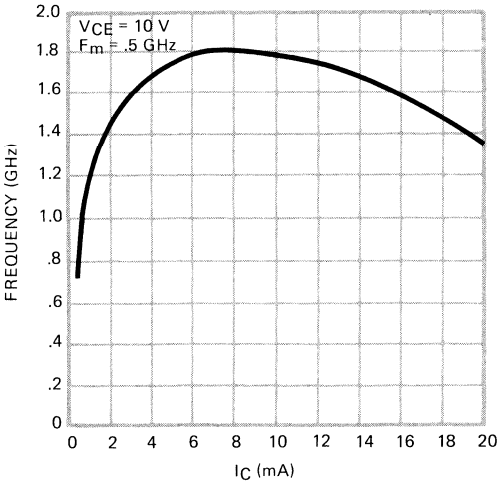
TYPICAL NOISE FIGURE VS COLLECTOR CURRENT



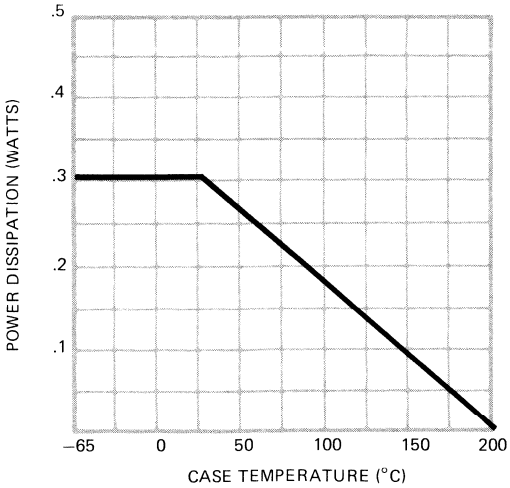
TYPICAL $|S_{21E}|^2$ VS COLLECTOR CURRENT



TYPICAL POWER OUTPUT @ 1 dB COMPRESSION VS COLLECTOR CURRENT

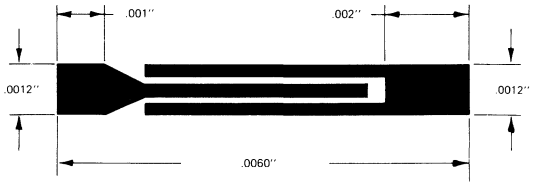


TYPICAL F_t VS COLLECTOR CURRENT



POWER DISSIPATION VS CASE TEMPERATURE

specification sheet



GEOMETRY 20

2N2857 JAN ELECTRICAL CHARACTERISTICS
(T_A = 25°C Unless Otherwise Specified)

Symbol	Definitions	Conditions	Min.	Typ.	Max.	Unit
C_{CB}	Collector to base feedback capacitance	V_{CB} = 10V, I_E = 0, f = 1.0 MHz	– – –	.6	1.0	pf
BV_{CEO}*	Collector-Emitter breakdown voltage	I_C = 3 mA	15	25	– – –	Vdc
BV_{CBO}	Collector-base breakdown voltage	I_C = 1 μA	30	47	– – –	Vdc
BV_{EBO}	Emitter-base breakdown voltage	I_E = 10 μA	3	5.5	– – –	Vdc
I_{CBO}	Collector to base cutoff current	V_{CB} = 15 Vdc	– – –	– – –	10	nA
h_{FE}	Forward-current transfer ratio	V_{CE} = 1 Vdc, I_C = 3 mA	30	100	150	– – –
V_{CE} (SAT)*	Collector-Emitter Voltage (saturated)	I_C = 10 mA, I_B = 1 mA	– – –	.2	.4	Vdc
V_{BE} (SAT)*	Base-Emitter Voltage (saturated)	I_C = 10 mA, I_B = 1 mA	– – –	.8	1.0	Vdc
I_{CES}*	Collector-Emitter Cutoff Current	V_{CE} = 16 Vdc	– – –	– – –	100	nA

*Applies to JANTX, JANTXV designated devices.
**Applies to non-JAN devices only.

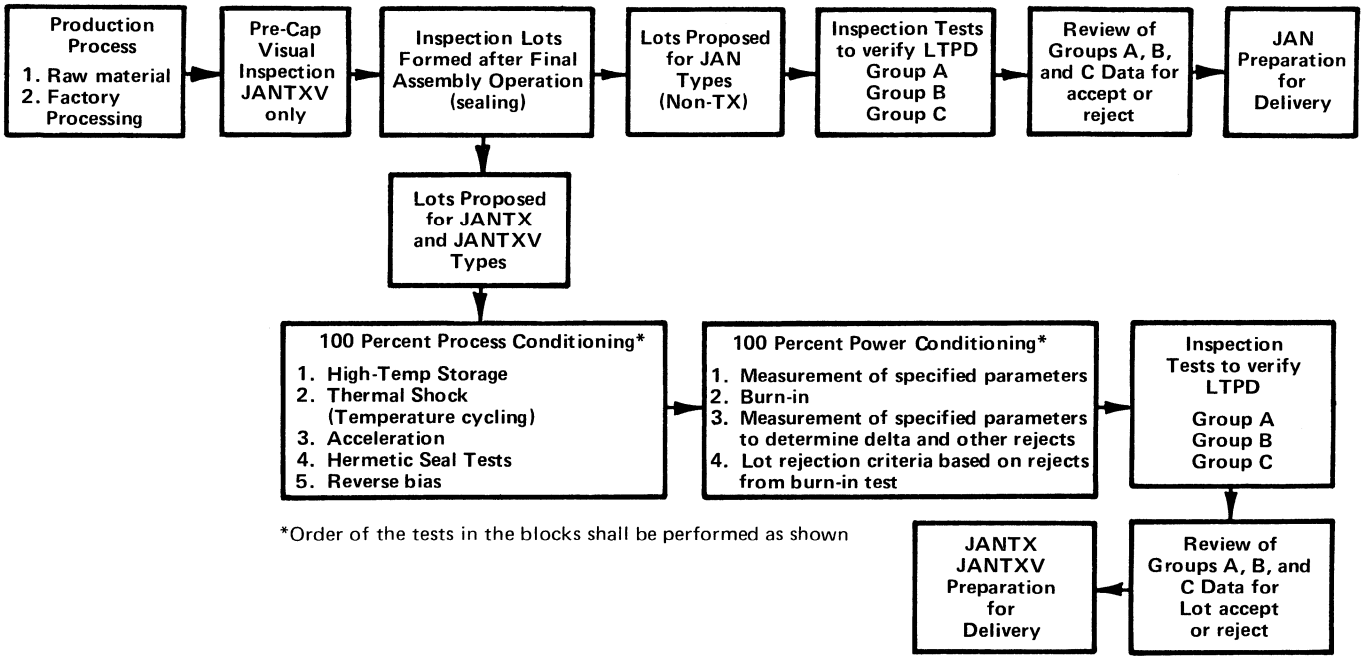
NOTE:
A selection of higher gain and lower noise figure devices are available upon special request.

MAXIMUM RATINGS
(Case Temperature 25°C unless otherwise noted)

Total Device Power Dissipation	ODS-509 (TO-72) 300mW
Collector Current	50 mA
Storage Temperature	–65 to +200°C
Hermeticity	5 x $(10)^{-8}$ Atm. cc/sec of He
Lead Temperature (soldering – 10 seconds each lead)	250°C

specification sheet

FLOW DIAGRAM FOR JAN (NON-TX), JANTX AND JANTXV TEST PROCEDURES



*Order of the tests in the blocks shall be performed as shown

100% PROCESS CONDITIONING PER MIL-STD-750 2N2857 JAN/TX/TXV

Test	Method	Conditions
Internal Inspection*	2072	————
High Temperature Life (Non-Operating, TX Types Only)	1031	Tstg = +200°C Time = 24 hours
Thermal Shock (Temperature Cycling)	1051	Test Condition C; 10 cycles; time at temperature extremes = 15 minutes minimum
Constant Acceleration	2006	20,000 G, in Y_1 orientation
Seal (Leak-Rate)	1071	Fine Leak: Condition G or H, maximum limit 1 x 10^{-7} Atm cc/sec. Gross Leak: Condition A, C, D, or F
High Temperature, Reverse Bias	————	V_{CB} = 15V, I_E = 0 time = 48 hours, T_A = +150°C Limit: I_{CBO} = 10 nA maximum at conclusion of test

100% POWER CONDITIONING PER MIL-STD-750 2N2857 JAN/TX/TXV

Test	Method	Conditions
Pre-burn in	————	Measure, Record I_{CES} and h_{FE}
Power Burn in	————	V_{CB} + 15V, P_T = 200 mW, T_A = +25°C ±3°C, Time = 168 hours
Post Burn in	————	ΔI_{CES} = +100% to −50% or 10 nA, whichever is greater Δh_{FE} = ± 15%

* Applies to JAN TXV designated devices only.

TEST CIRCUITS

NOTES:

1. Neutralization procedure
   A. Connect a 450 MHz signal generator (with Z_{out} = 50 ohms) to the input terminals of the amplifier.
   B. Connect a 50 ohm RF voltmeter across the output terminals of the amplifier.
   C. Apply V_{EE}, and with the signal generator adjusted for 10 mV output, tune C_1, C_3 and C_4 for maximum output.
   D. Interchange the connection to the signal generator and the output indicator.
   E. With sufficient signal applied to the output terminals of the amplifier, adjust C_2 for a minimum indication at the input.
   F. Repeat steps A, B and C to determine if retuning
2. L_1 and L_2 — Silver-plated brass rod, 1.50" (38.10 mm) long x .25" (6.35 mm) diameter. Install at least .50" (12.70 mm) from nearest vertical chassis surface. Tap 1.25" (31.75 mm) from chassis end. face. Tap 1.25 (31.75 mm) from chassis end.
3. External interlead shield to isolate the collector lead from the emitter and base leads.

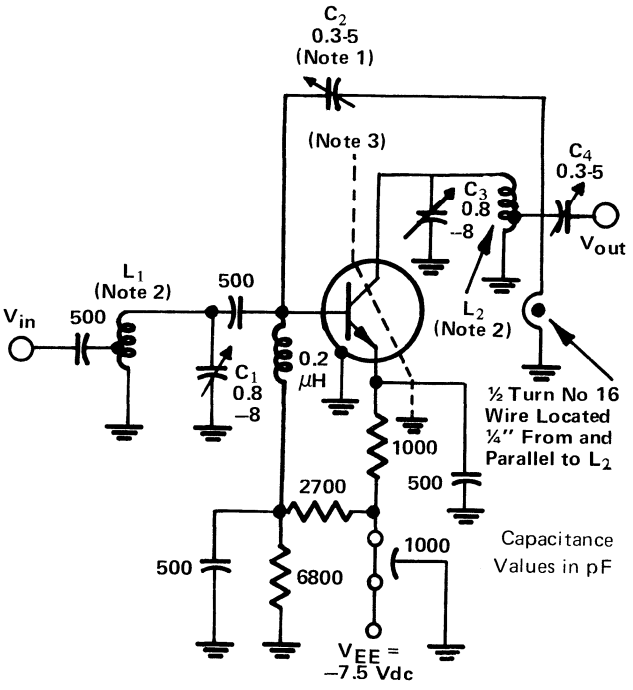


FIGURE 1. SMALL-SIGNAL POWER GAIN TEST CIRCUIT

PROCEDURE:

1. With a short circuit applied between the collector and emitter terminals adjust 31.9 MHz input for 0.5 volt RMS at emitter terminal of transistor.
2. After removing the short circuit between the collector and emitter circuit insert unit to be tested and adjust V_{CC} and V_{EE} for V_{CB} = 6 Vdc I_E = 2 mAdc.
3. Read $r_b'C_c$ on RF voltmeter scale ($r_b'C_c$ in picoseconds = 10 times meter indication in millivolts) (1 millivolt = 10 picoseconds).
4. External interlead shield to isolate the collector lead from the emitter and base leads.

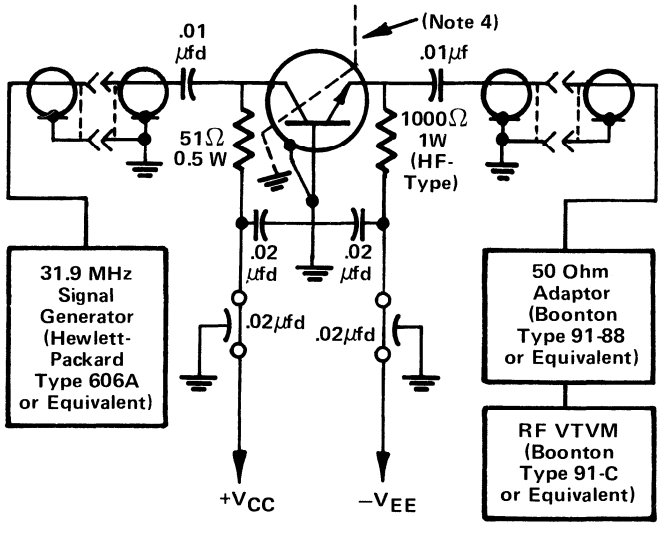
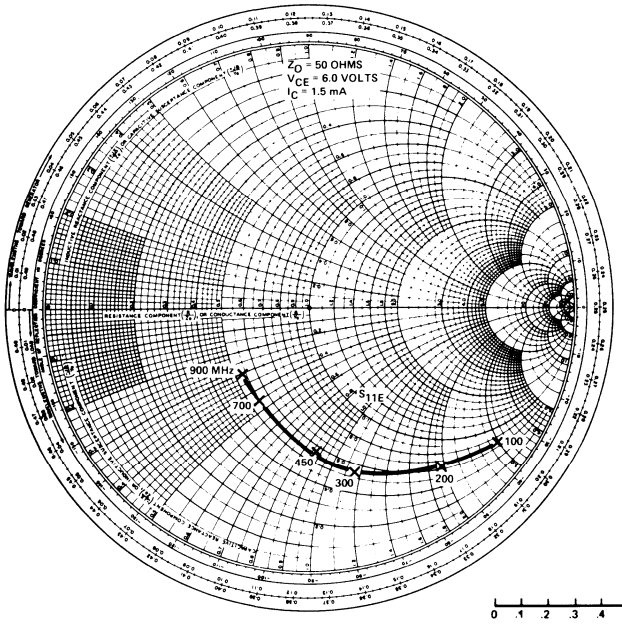
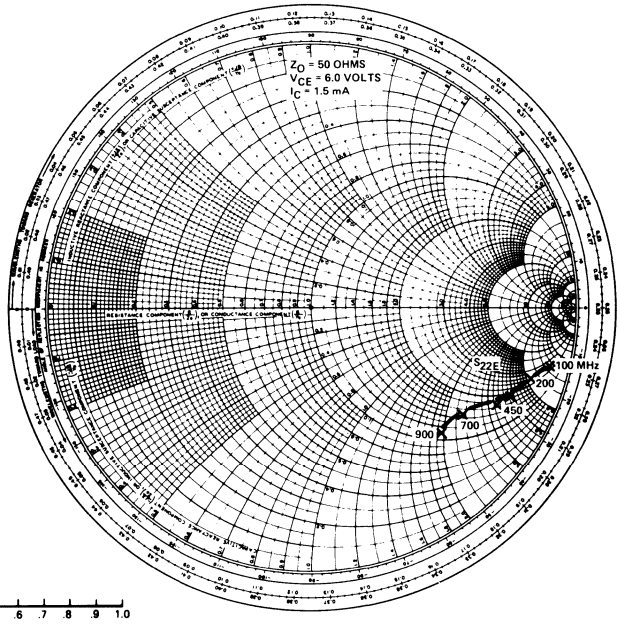


FIGURE 2. COLLECTOR-BASE TIME CONSTANT TEST CIRCUIT

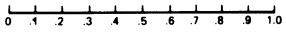
specification sheet



TYPICAL S_{11E} VS FREQUENCY



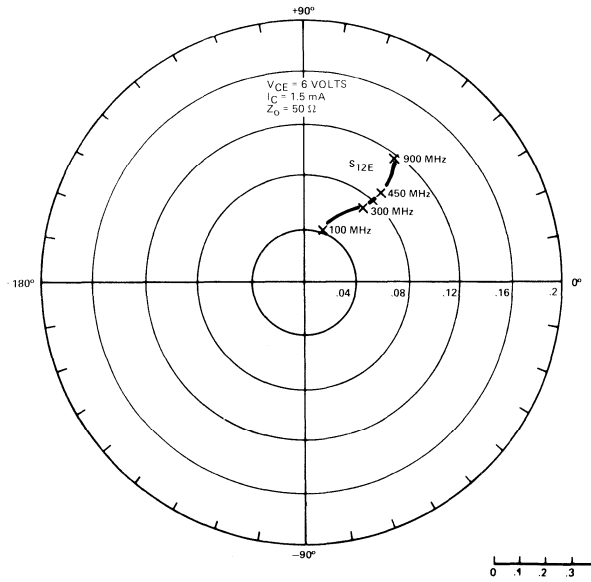
TYPICAL S_{22E} VS FREQUENCY



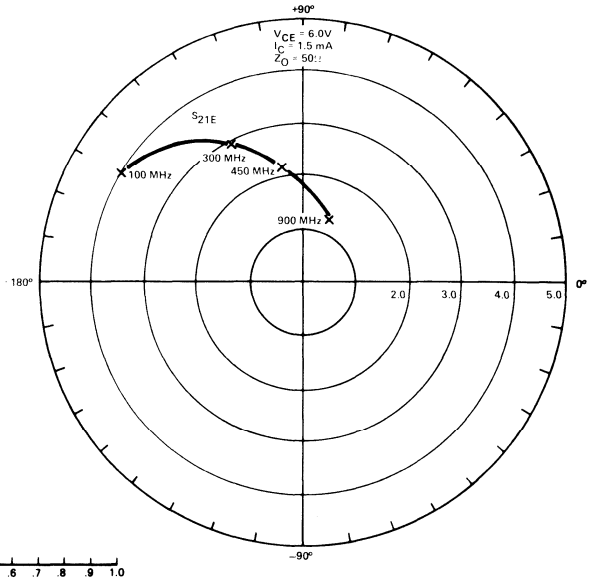
2N2857 JAN
TYPICAL COMMON EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 6.0 VOLTS, $Z_G = Z_L$ = 50 Ω

FREQUENCY (MHz)	COLLECTOR CURRENT (mA)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
		$\|S_{11E}\|$	ϕS_{11E}	$\|S_{21E}\|$	ϕS_{21E}	$\|S_{12E}\|$	ϕS_{12E}	$\|S_{22E}\|$	ϕS_{22E}
100	1.0	.91	−26°	3.2	152°	.04	73°	.96	−11°
	1.5	.88	−39°	3.9	149°	.04	71°	.95	−12°
	3.0	.75	−48°	6.5	136°	.04	70°	.89	−15°
	5.0	.67	−53°	8.2	128°	.03	69°	.84	−16°
200	1.0	.82	−43°	3.0	138°	.06	65°	.92	−16°
	1.5	.77	−48°	3.6	135°	.06	65°	.92	−16°
	3.0	.61	−65°	5.4	122°	.05	61°	.82	−18°
	5.0	.49	−77°	6.4	114°	.04	60°	.78	−18°
300	1.0	.69	−64°	2.5	120°	.08	54°	.89	−21°
	1.5	.63	−70°	3.0	117°	.07	52°	.84	−23°
	3.0	.45	−89°	4.0	105°	.06	55°	.76	−22°
	5.0	.37	−100°	4.5	99°	.06	58°	.72	−21°
400	1.0	.62	−76°	2.3	110°	.09	51°	.84	−25°
	1.5	.56	−81°	2.6	108°	.09	50°	.81	−26°
	3.0	.39	−100°	3.9	97°	.07	56°	.79	−24°
	5.0	.32	−111°	3.7	91°	.06	60°	.71	−23°
450	1.0	.56	−80°	2.1	107°	.09	49°	.84	−26°
	1.5	.55	−86°	2.2	102°	.08	51°	.80	−26°
	3.0	.39	−104°	2.8	92°	.07	55°	.74	−25°
	5.0	.32	−117°	3.4	87°	.06	60°	.72	−23°
500	1.0	.54	−87°	2.0	101°	.10	49°	.82	−28°
	1.5	.49	−93°	2.2	97°	.09	50°	.78	−28°
	3.0	.34	−112°	2.8	87°	.08	56°	.73	−26°
	5.0	.29	−123°	3.0	83°	.07	61°	.70	−24°
600	1.0	.46	−102°	1.7	91°	.11	47°	.77	−31°
	1.5	.41	−108°	1.9	88°	.10	49°	.74	−31°
	3.0	.30	−126°	2.3	79°	.09	57°	.70	−28°
	5.0	.26	−138°	2.5	76°	.09	63°	.68	−26°
700	1.0	.44	−111°	1.6	85°	.11	47°	.72	−34°
	1.5	.38	−117°	1.8	83°	.11	50°	.72	−33°
	3.0	.29	−135°	2.1	75°	.10	60°	.68	−30°
	5.0	.25	−145°	2.2	70°	.09	64°	.67	−28°

NOTE: Full S-Parameter measurements on an individual unit basis are available at a nominal charge.



TYPICAL S_{12E} VS FREQUENCY



TYPICAL S_{21E} VS FREQUENCY

2N2857 JAN
TYPICAL COMMON EMITTER Y-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 6.0 VOLTS, MAGNITUDE IN MILLI-MHOS

FREQUENCY (MHz)	I_C (mA)	INPUT ADMITTANCE		FORWARD TRANSFER ADMITTANCE		REVERSE TRANSFER ADMITTANCE		OUTPUT ADMITTANCE	
		Y_{ie}	ϕ_{yie}	Y_{fe}	ϕ_{ie}	Y_{re}	ϕ_{yre}	Y_{oe}	ϕ_{yoe}
100	1.0	3.9	78°	34.7	−12°	0.48	−92°	1.2	84°
	1.5	5.1	76°	43.8	−12°	0.48	−90°	1.2	84°
	3.0	7.2	67°	82.1	−20°	0.50	−86°	1.1	78°
	5.0	8.1	63°	110.9	−27°	0.46	−87°	1.2	73°
200	1.0	6.9	74°	35.9	−17°	0.72	−90°	1.8	84°
	1.5	7.7	72°	44.6	−18°	0.72	−92°	1.8	83°
	3.0	10.6	61°	81.0	−29°	0.72	−90°	1.8	80°
	5.0	12.9	53°	108.4	−38°	0.73	−91°	1.7	80°
300	1.0	11.0	69°	35.1	−26°	1.1	−92°	2.7	89°
	1.5	12.0	66°	44.8	−29°	1.1	−94°	2.9	84°
	3.0	15.5	51°	74.3	−43°	1.1	−93°	2.8	83°
	5.0	17.4	43°	91.5	−52°	1.1	−92°	2.8	82°
400	1.0	13.5	66°	35.7	−31°	1.4	−91°	3.4	87°
	1.5	14.6	61°	44.1	−35°	1.4	−93°	3.5	85°
	3.0	17.9	46°	69.1	−50°	1.4	−91°	3.4	83°
	5.0	19.4	38°	82.6	−60°	1.3	−91°	3.4	82°
450	1.0	14.9	60°	35.7	−35°	1.4	−93°	3.8	85°
	1.5	16.2	60°	39.5	−39°	1.4	−90°	3.8	81°
	3.0	19.7	45°	61.0	−55°	1.4	−92°	3.9	78°
	5.0	21.2	37°	78.3	−64°	1.4	−91°	3.7	80°
500	1.0	16.4	59°	35.3	−40°	1.7	−92°	4.1	85°
	1.5	17.6	56°	42.3	−44°	1.7	−91°	4.2	82°
	3.0	20.4	40°	62.4	−61°	1.7	−92°	4.2	82°
	5.0	21.7	33°	71.2	−70°	1.7	−92°	4.1	81°
600	1.0	20.1	53°	35.9	−48°	2.2	−93°	5.0	82°
	1.5	21.0	48°	42.2	−54°	2.1	−93°	5.1	81°
	3.0	22.8	34°	57.3	−70°	2.1	−93°	4.9	82°
	5.0	23.4	27°	63.4	−79°	2.1	−92°	4.8	81°
700	1.0	22.3	50°	37.2	−54°	2.5	−92°	5.7	79°
	1.5	22.8	44°	42.5	−59°	2.5	−92°	5.7	81°
	3.0	24.0	30°	55.1	−75°	2.5	−91°	5.4	81°
	5.0	24.3	24°	59.9	−85°	2.5	−91°	5.4	81°

NOTE.

1. These parameters have been calculated from S-parameter data measured on a computer controlled network analyzer.

specification sheet

2N2857 JAN
TYPICAL COMMON EMITTER H-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 6.0 VOLTS

FREQUENCY (MHz)	I_C (mA)	SHORT CIRCUIT INPUT IMPEDANCE		FORWARD CURRENT TRANSFER RATIO		REVERSE VOLTAGE TRANSFER RATIO		OPEN CIRCUIT OUTPUT ADMITTANCE	
		h_{ie}[2]	ϕ_{hie}	h_{fe}	ϕ_{hfe}	h_{re}	ϕ_{hre}	h_{oe}[2]	ϕ_{oe}
100	1.0	254	−78°	8.8	− 91°	.122	10°	4.5	14°
	1.5	195	−76°	8.6	− 88°	.094	13°	4.4	17°
	3.0	137	−67°	11.3	− 88°	.069	25°	6.0	15°
	5.0	122	−63°	13.5	− 90°	.057	29°	6.8	12°
200	1.0	144	−74°	5.2	− 92°	.103	14°	4.2	23°
	1.5	129	−72°	5.8	− 91°	.093	15°	4.6	20°
	3.0	93	−61°	7.6	− 91°	.067	27°	5.9	15°
	5.0	77	−53°	8.3	− 91°	.056	35°	6.5	12°
300	1.0	90	−69°	3.2	− 95°	.107	18°	4.3	30°
	1.5	82	−66°	3.7	− 95°	.092	19°	4.9	28°
	3.0	64	−51°	4.8	− 94°	.075	35°	6.2	19°
	5.0	57	−43°	5.2	− 95°	.067	43°	6.6	16°
400	1.0	73	−66°	2.6	− 98°	.108	22°	4.8	34°
	1.5	68	−61°	3.0	− 97°	.098	25°	5.3	31°
	3.0	55	−46°	3.8	− 97°	.080	41°	6.3	23°
	5.0	51	−38°	4.2	− 98°	.072	49°	6.7	20°
450	1.0	67	−60°	2.4	− 96°	.097	25°	4.9	41°
	1.5	61	−60°	2.4	− 99°	.092	29°	5.2	37°
	3.0	50	−45°	3.0	−100°	.072	42°	5.8	29°
	5.0	47	−37°	3.6	−101°	.066	51°	6.2	23°
500	1.0	60	−59°	2.1	− 99°	.106	28°	5.2	40°
	1.5	56	−56°	2.4	−101°	.098	31°	5.6	35°
	3.0	48	−40°	3.0	−102°	.084	47°	6.3	27°
	5.0	45	−33°	3.3	−103°	.079	54°	8.5	23°
600	1.0	49	−53°	1.8	−101°	.110	33°	6.0	42°
	1.5	47	−48°	2.0	−102°	.103	38°	6.3	38°
	3.0	43	−34°	2.5	−105°	.096	52°	6.6	28°
	5.0	42	−27°	2.7	−106°	.093	60°	6.9	25°
700	1.0	44	−50°	1.7	−104°	.114	38°	6.7	40°
	1.5	43	−44°	1.8	−104°	.111	43°	6.9	38°
	3.0	41	−30°	2.2	−106°	.105	57°	7.2	29°
	5.0	41	−24°	2.4	−109°	.103	64°	7.3	26°

NOTE:
1. These parameters have been calculated from S-parameter data measured on a computer controlled network analyzer.
2. The magnitude of h_{ie} is in ohms, the magnitude of h_{oe} is in millimhos.

specification sheet

npn silicon planar transistors

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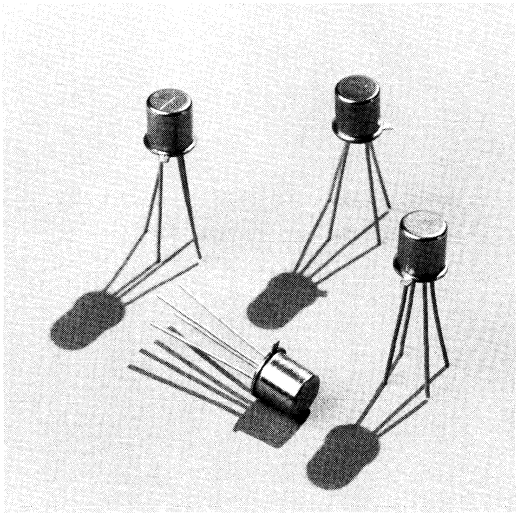
FEATURES

- LOW NOISE FIGURE – 1.0 dB MAX AT 60 MHz
- LARGE DYNAMIC RANGE – +23 dBm 1-dB COMPRESSION
- GOLD METALLIZATION
- GUARANTEED S-PARAMETER SPECIFICATIONS
- LOW COST
- HIGH RELIABILITY
- JEDEC REGISTERED

DESCRIPTION

The 2N6665 transistor is designed for low noise operation in the 10 to 700 MHz frequency range. This transistor exhibits a low noise figure over a large collector current range resulting in low noise, wide dynamic range performance. Features include a guaranteed S-Parameter window specification, minimum high frequency h_{fe}, and standard noise figure test circuit. The 2N6665 finds wide application in sophisticated radar and communications equipment at VHF/UHF.



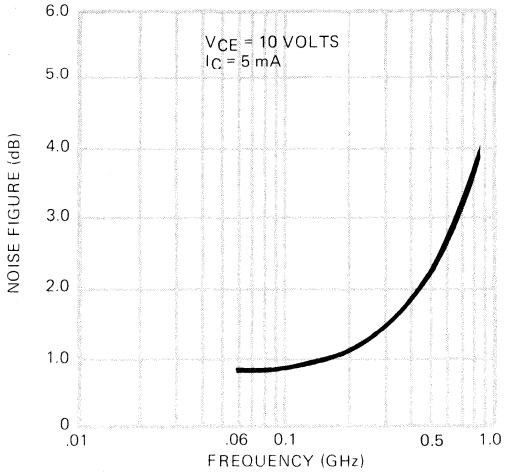
APPLICATIONS

IF, RF amplifiers.

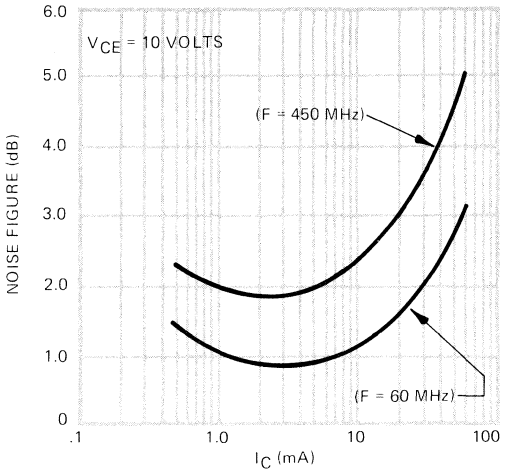
2N6665 R.F. SPECIFICATIONS

Symbol	Definition	Conditions	Min.	Max.	Units
$\lvert h_{fe} \rvert$	Magnitude of small-signal Short-circuit forward current transfer ratio	V_{CE} = 10 V I_C = 5 mA F = 110 MHz	9	——	——
G_{op}	Small-signal insertion power gain @ minimum Noise Figure	V_{CE} = 10 V I_C = 5 mA F = 60 MHz Figure 1	22.0	32.0	dB
BW_{op}	Bandwidth, BW at minimum Noise Figure	V_{CE} = 10 V I_C = 5 mA	3.0	10.0	MHz
N.F.	Spot Noise Figure	V_{CE} = 10 V I_C = 5 mA F = 60 MHz Figure 1	——	1.0	dB

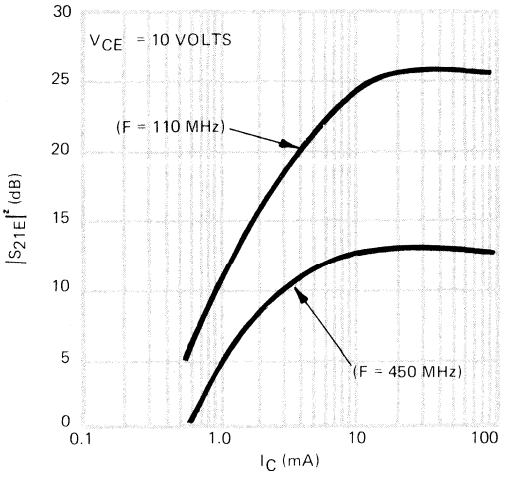
specification sheet



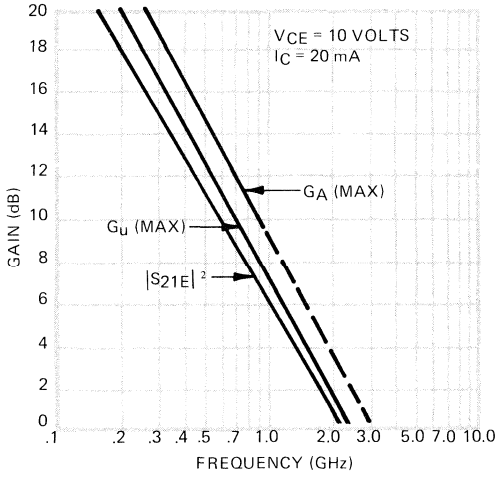
TYPICAL NOISE FIGURE VS FREQUENCY



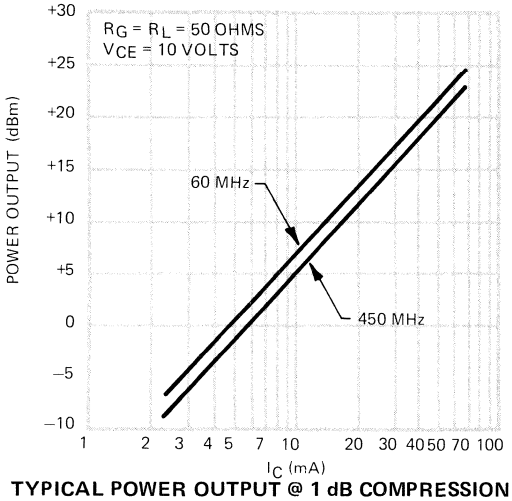
TYPICAL NOISE FIGURE VS COLLECTOR CURRENT



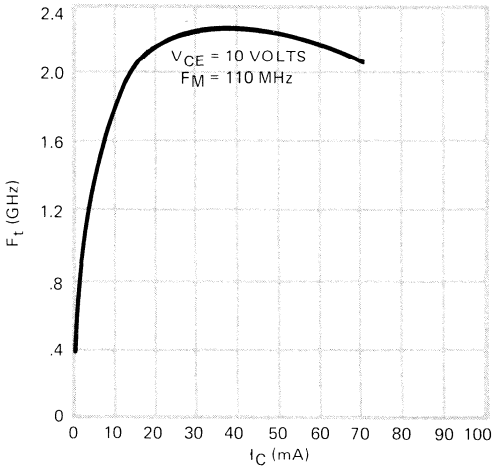
TYPICAL GAIN $|S_{21E}|^2$ VS COLLECTOR CURRENT



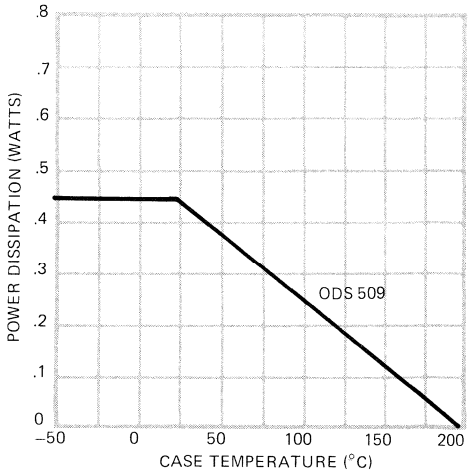
2N6665 GAIN PARAMETERS VS FREQUENCY



TYPICAL POWER OUTPUT @ 1 dB COMPRESSION POINT VS COLLECTOR CURRENT



TYPICAL F_T VS COLLECTOR CURRENT



POWER DISSIPATION VS CASE TEMPERATURE

specification sheet

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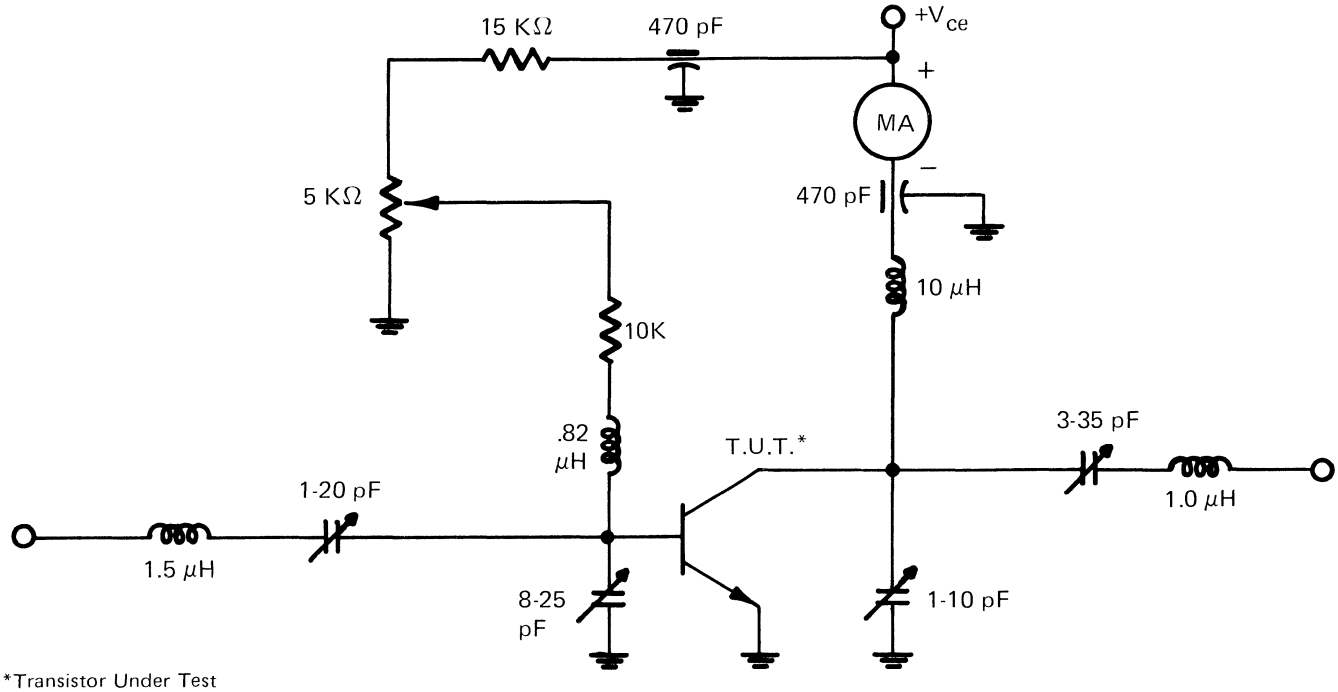

*Transistor Under Test

FIGURE 1. 60 MHz N.F. AND GAIN TEST CIRCUIT

S-PARAMETER LIMITS[1]

Description	Symbol	V_{CE} = 10V, I_C = 5 mA, 110 MHz		V_{CE} = 10 V, I_C = 20 mA, 500 MHz	
		Min.	Max.	Min.	Max.
Common-Emitter Input Reflection Coefficient	$\|S_{11}\|$	.60	.75	.30	.45
	ϕS_{11}	−70°	−100°	−170°	+168
Common-Emitter Forward Transmission Coefficient	$\|S_{21}\|$	7.5	9.5	3.0	4.5
	ϕS_{21}	+115°	+135°	+65°	+80°
Common-Emitter Reverse Transmission Coefficient	$\|S_{12}\|$	.035	.060	.080	.115
	ϕS_{12}	+40°	+65°	+65°	+75°
Common-Emitter Output Reflection Coefficient	$\|S_{22}\|$	.65	.85	.35	.55
	ϕS_{22}	−16°	−31°	−24°	−36°

Note 1. 50 ohm Scattering Parameters

Circuit Conditions — tested in a 50 ohm system, common emitter case grounded configuration employing a test fixture with less than 1.2:1 VSWR at input and output ports. T_A = +25°C ±3°C.

specification sheet

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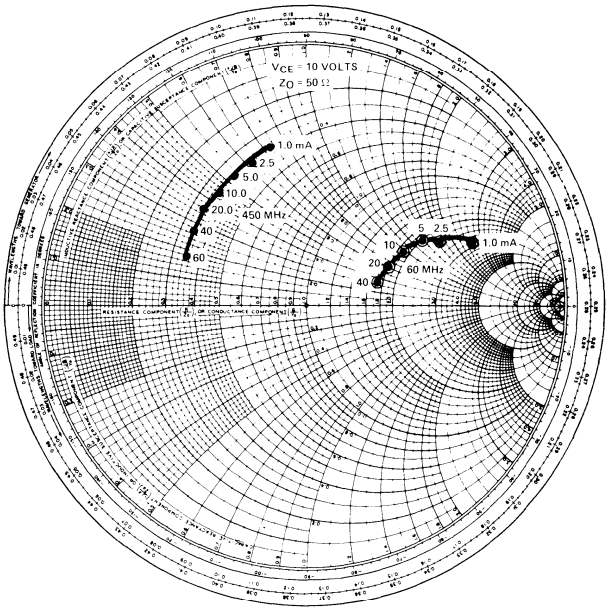
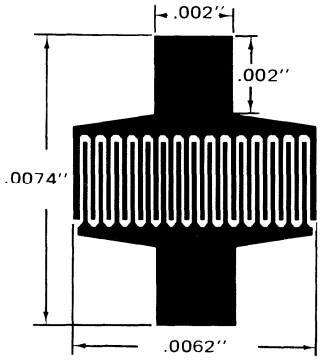


TYPICAL OPTIMUM GENERATOR IMPEDANCE VS COLLECTOR CURRENT



GEOMETRY 60

ELECTRICAL CHARACTERISTICS (25°C Ambient Temperature unless otherwise noted)

Symbol	Definition	Conditions	Min.	Typ.	Max.
BV_{CBO}	Collector base Breakdown voltage	I_C = 10 μA	20 V		
BV_{EBO}	Emitter base breakdown voltage	I_E = 10 μA	2.5 V	3.0 V	
I_{CBO}	Collector cut off current	V_{CB} = 10 V			10 nA
h_{FE}	Current transfer ratio	V_{CE} = 10V, I_C, 5 mA	20		300
C_{CB}	Output Capacitance	V_{CB} = 15 V I_E = 0, F = 1 MHz			1.7 pF

MAXIMUM RATING
(Case Temperature 25°C unless otherwise noted)

Total Device Power	509 Case – 450 mW
V_{CBO} Collector to Base Voltage	20 V
V_{EBO} Emitter to Base Voltage	2.5 V
Collector Current	125 mA
Storage Temperature	–65 to +200°C
Hermeticity	5 x $(10)^{-8}$ cc/sec of He
Operation Junction Temperature	+200°C
Lead Temperature (Soldering – 10 Seconds each lead)	230°C

ENVIRONMENTAL RATINGS PER MIL-STD-750

	Method	Level
Storage Temperature	1031	–65 to +200°C
Temperature Cycle	1051	10 cycles –65 to +200°C
Shock	2016	500 g's
Vibration	2056	15 g's
Constant Acceleration	2006	20,000 g's
Humidity	1021	10 days

specification sheet

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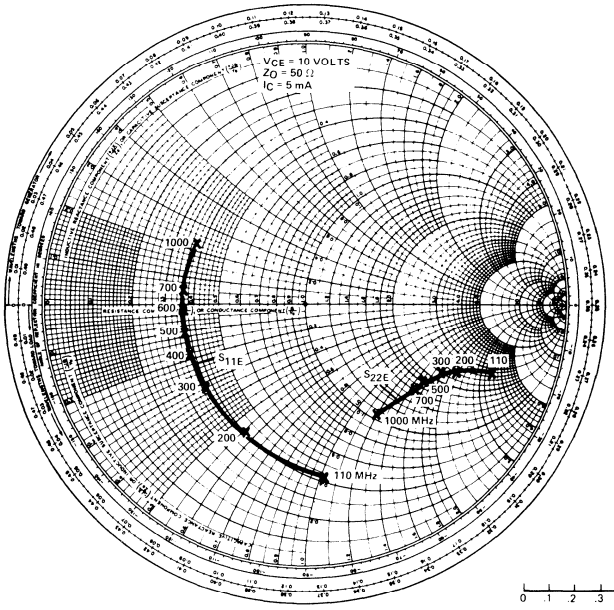
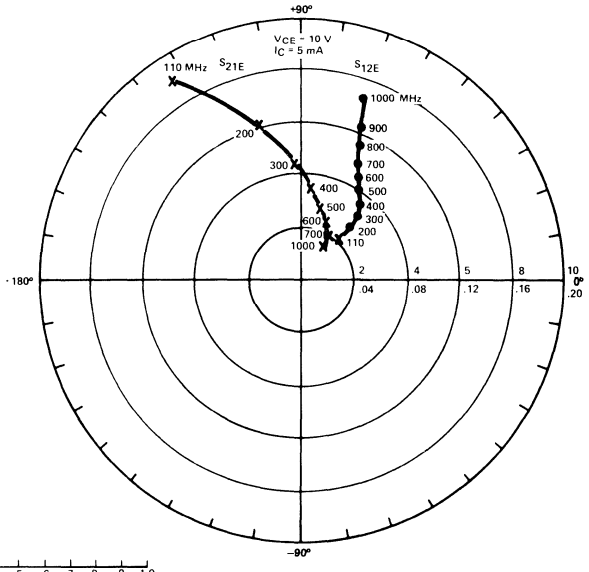


TYPICAL S_{11E} AND S_{22E} VS FREQUENCY



TYPICAL S_{21E} AND S_{12E} VS FREQUENCY

2N6665
TYPICAL COMMON-EMITTER S-PARAMETERS AT 25°C LEAD TEMPERATURE
V_{CE} = 10 VOLTS, $Z_G = Z_L = 50\ \Omega$

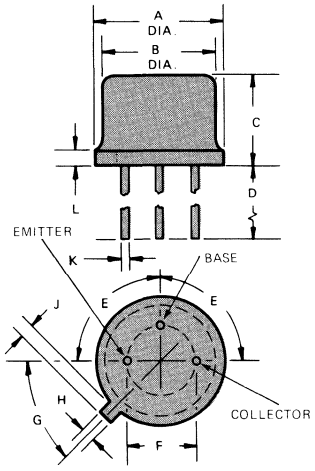
FREQUENCY (MHz)	COLLECTOR CURRENT (mA)	INPUT REFLECTION COEFFICIENT		FORWARD TRANSMISSION COEFFICIENT		REVERSE TRANSMISSION COEFFICIENT		OUTPUT REFLECTION COEFFICIENT	
		$\lvert S_{11E}\rvert$	ϕS_{11E}	$\lvert S_{21E}\rvert$	ϕS_{21E}	$\lvert S_{12E}\rvert$	ϕS_{12E}	$\lvert S_{22E}\rvert$	ϕS_{22E}
110.0	5	.667	−83.6°	8.740	122.6°	.040	48.9°	.765	−21.7°
	20	.429	−116.4°	13.093	105.9°	.028	55.1°	.560	−23.7°
200.0	5	.551	−116.0°	6.026	104.7°	.054	45.7°	.649	−25.8°
	20	.381	−142.6°	8.057	92.8°	.041	60.3°	.481	−24.5°
300.0	5	.496	−138.8°	4.324	92.4°	.064	48.1°	.597	−28.4°
	20	.365	−158.9°	5.605	84.4°	.062	64.4°	.460	−26.4°
400.0	5	.475	−155.0°	3.455	83.1°	.070	50.9°	.578	−30.7°
	20	.364	−170.4°	4.387	76.9°	.074	65.6°	.456	−27.9°
500.0	5	.466	−167.2°	2.798	75.0°	.080	55.8°	.570	−32.4°
	20	.367	−178.8°	3.521	70.4°	.091	67.0°	.455	−29.2°
600.0	5	.467	−178.2°	2.388	69.1°	.088	59.9°	.551	−35.6°
	20	.373	173.9°	2.992	65.1°	.106	67.3°	.446	−30.6°
700.0	5	.470	174.0°	2.131	62.1°	.098	63.3°	.528	−38.6°
	20	.384	167.7°	2.652	59.0°	.121	67.4°	.427	−32.7°
800.0	5	.474	167.0°	1.878	57.3°	.114	65.4°	.511	−44.3°
	20	.392	163.7°	2.337	54.1°	.138	67.0°	.409	−37.4°
900.0	5	.469	161.1°	1.726	52.4°	.127	67.1°	.506	−50.4°
	20	.394	158.6°	2.131	50.0°	.152	66.2°	.406	−44.4°
1000.0	5	.464	153.6°	1.582	46.3°	.145	70.0°	.503	−56.4°
	20	.391	152.4°	1.953	44.1°	.169	67.0°	.410	−50.6°

notes

outline drawings

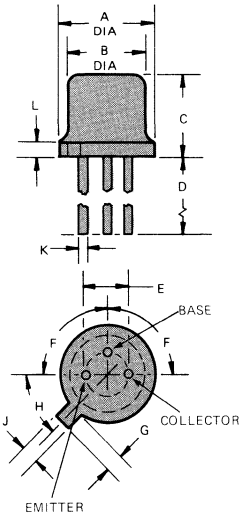
ODS 506

DIM.	INCHES MIN.	INCHES MAX.	MM MIN.	MM MAX.
A	0.350	0.370	8,89	9,40
B	0.315	0.335	8,00	8,51
C	0.240	0.260	6,10	6,60
D	0.500	– –	12,70	– –
E	89°	91°	89°	91°
F	0.190	0.210	4,83	5,33
G	43°	47°	43°	47°
H	0.028	0.034	0,71	0,86
J	0.029	0.043	0,74	1,09
K	0.016	0.021	0,41	0,53
L	– –	0.040	– –	1,02



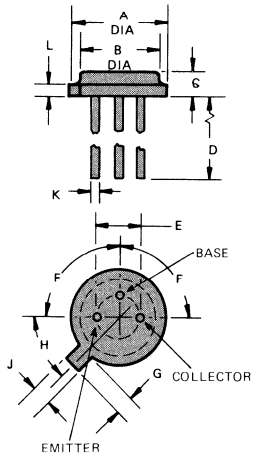
ODS 507

DIM.	INCHES MIN.	INCHES MAX.	MM MIN.	MM MAX.
A	0.209	0.230	5,31	5,84
B	0.178	0.195	4,52	4,95
C	0.170	0.210	4,32	5,33
D	0.500	– –	12,70	– –
E	0.090	0.110	2,29	2,79
F	89°	91°	89°	91°
G	0.028	0.048	0,71	1,22
H	43°	47°	43°	47°
J	0.036	0.046	0,91	1,17
K	0.016	0.021	0,41	0,53
L	– –	0.030	– –	0,76



ODS 508

DIM.	INCHES MIN.	INCHES MAX.	MM MIN.	MM MAX.
A	0.209	0.230	5,31	5,84
B	0.178	0.195	4,52	4,95
C	0.065	0.085	1,65	2,16
D	0.500	– –	12,70	– –
E	0.090	0.110	2,29	2,79
F	89°	91°	89°	91°
G	0.028	0.048	0,71	1,22
H	43°	47°	43°	47°
J	0.036	0.046	0,91	1,17
K	0.016	0.021	0,41	0,53
L	– –	0.030	– –	0,76



outline drawings

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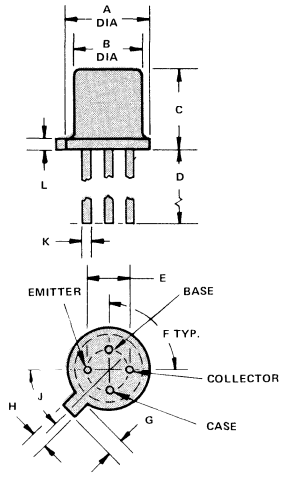
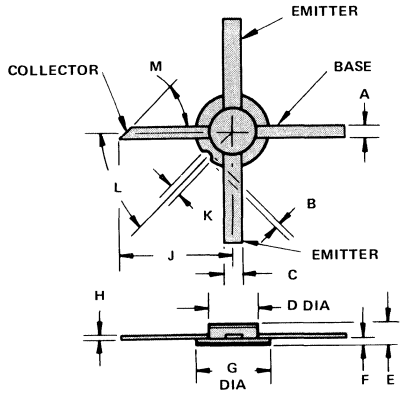


ODS 509

DIM.	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
A	0.209	0.230	5,31	5,84
B	0.178	0.195	4,52	4,95
C	0.170	0.210	4,32	5,33
D	0.500	– –	12,70	– –
E	0.090	0.110	2,29	2,79
F	89°	91°	89°	91°
G	0.028	0.048	0,71	1,22
H	0.036	0.046	0,91	1,17
J	43°	47°	43°	47°
K	0.016	0.019	0,41	0,48
L	– –	.020	– –	0,51

NOTE: REVERSE THE EMITTER AND BASE LEAD DESIGNATION FOR THE MA-42150 AND MA-42190 SERIES FOR ODS 510, 511 AND 512 PACKAGES (COMMON-BASE CONFIGURATION).

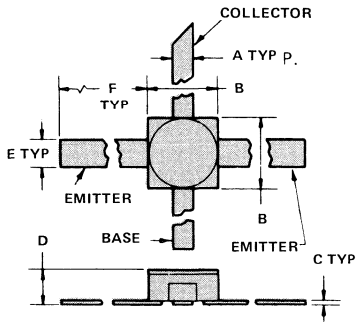


ODS 510

DIM.	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
A	0.024	0.036	0,61	0,91
B	0.015 REF.		0,38 REF.	
C	0.054	0.066	1,37	1,68
D	0.129	0.141	3,10	3,40
E	0.043	0.063	1,09	1,60
F	0.016	0.024	0,41	0,61
G	0.195	0.215	4,95	5,46
H	0.0015	0.0045	0,038	0,114
J	0.279	0.321	7,09	8,15
K	0.030 REF.		0,76 REF.	
L	40° REF.		40° REF.	
M	45° REF.		45° REF.	

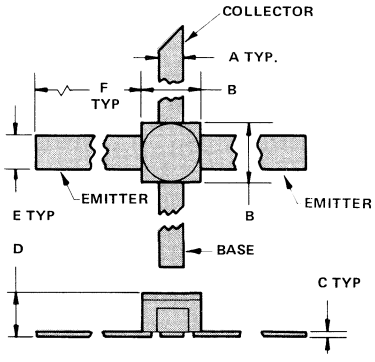
ODS 511

DIM.	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
A	0.016	0.024	0,41	0,61
B	0.095	0.105	2,41	2,67
C	0.002	0.006	0,05	0,15
D	— —	0.050	— —	1,27
E	0.036	0.044	0,91	1,12
F	0.190	0.260	5,84	7,11



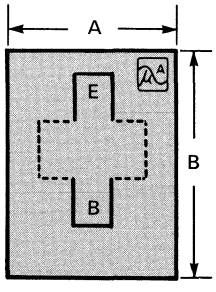
ODS 512

DIM.	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
A	0.016	0.024	0,41	0,61
B	0.065	0.075	1,65	1,91
C	0.002	0.006	0,05	0,15
D	— —	0.050	— —	1,27
E	0.036	0.044	0,91	1,12
F	0.230	0.280	5,84	7,11



ODS 520 (NOMINAL CHIP DIMENSIONS)

MODEL	DIM. (MILS)	
	A	B
MA-42000	13	13
MA-42020	16	16
MA-42050	15	15
MA-42110	13	13
MA-42120	15	15
MA-42140	15	15
MA-42150	15	15
MA-42160	15	15
MA-42180	24	29
MA-42190	24	29
2N2857	16	16
2N6665	13	13



appendices

appendices
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